WEST

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Search Results -

Terms	Documents
L6 and (generat$ or creat$ or regenerat$ or modif$ or change$ or recreat$ or author$)	19

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L7

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Search History

DATE: Friday, September 27, 2002 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=TDBD; PLUR=YES; OP=OR		
L7	L6 and (generat$ or creat$ or regenerat$ or modif$ or change$ or recreat$ or author$)	19	L7
L6	L4 and (access$ or avail$ or entry$ or share$)	28	L6
L5	L4 and (syntax$ or language$ or syntact$ or schema$)	6	L5
L4	L2 and (drop$ or end or ends or ended or ending or kill$)	44	L4
L3	L2 adj3 (syntax or syntact$ or language$ or schema$)	0	L3
L2	L1 adj2 (table$ or graph$ or chart$ or tupl$ or matrix$ or matrice$)	171	L2
L1	persistent or resident or memory or sram or ram or tsr	11829	L1

END OF SEARCH HISTORY

WEST

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Search Results - Record(s) 1 through 6 of 6 returned.

☐ 1. Document ID: NN9408169

L5: Entry 1 of 6 File: TDBD Aug 1, 1994

TDB-ACC-NO: NN9408169

DISCLOSURE TITLE: Sizing of Textual Elements for National Language Support

L5: Entry 1 of 6 File: TDBD Aug 1, 1994

DOCUMENT-IDENTIFIER: NN9408169
TITLE: Sizing of Textual Elements for National Language Support

Disclosure Title (1):
Sizing of Textual Elements for National Language Support

Disclosure Text (1):
Described is a method which assists translation of text strings from English to other National Languages which need expansion in string length; in particular German. An in-memory table provides a set of recommended text size increases for various lengths of text strings. - A screen-panel development tool can use the table in various ways: either to automatically increase field lengths or to give warnings to the developer thus avoiding tedious resizing following language translation. - A problem when developing applications that allow for easy translation of user interface text is that it is best to allow extra space for translation to more verbose languages. For example, the German translation of an English string might be 30% longer. If the control/window was not large enough, the end of the German text may not be visible. Developers must therefore arrange panels etc so that there is enough space for the translations. This can be difficult because the amount of extra space would vary with the size of the string and the font being used. One problem is the fact that some fields may not be large enough to allow for the translation and the developer may not realise this until the translation is being done. Another is that in order to size the fields correctly the developer has to size each field which will require calculating the extra space required and adding that to the existing size for every text field. - Part of the solution is to maintain in PMGUIDE/2 memory the table of recommended size increases for given lengths of strings. The solution to the first problem would be to have a piece of program code perform the checking on each text control/window (element) by querying the space required to display the current text using the current font, and then to warn the developer if the element is not large enough. The second solution is to automatically resize the text elements (eg static text, radio buttons, checkboxes, groupboxes, pushbuttons, windows ...) by performing the same querying step, and then increasing the size of the element based on the table held in memory. For example, the table might contain the following: 0 < N < 10 increase by 30% 10 = < N < 20 increase by 50% etc. - where N = No. of characters. - The table would be configurable and therefore allow easy regeneration of panel definitions. The developer (user of PMGUIDE/2) would just have to ensure that all of the window is visible and that none of the controls overlap. - The invention ensures that the panel developer does not forget the necessary expansion because the panel

development tool uses the table to expand or warn automatically.

2. Document ID: NN9311629

L5: Entry 2 of 6 File: TDBD Nov 1, 1993

TDB-ACC-NO: NN9311629

DISCLOSURE TITLE: National Language Support Enablement for Culture-Specific Operations

L5: Entry 2 of 6 File: TDBD Nov 1, 1993

DOCUMENT-IDENTIFIER: NN9311629
TITLE: National Language Support Enablement for Culture-Specific Operations

Disclosure Title (1):
National Language Support Enablement for Culture-Specific Operations

Disclosure Text (1):
This document contains drawings, formulas, and/or symbols that will not appear on line. Request hardcopy from ITIRC for complete article. Figure 1. Organizational Structure Disclosed is an architecture for performing culture specific operations on parameters that are inserted into text strings as part of National Language Support (NLS) enablement of a software product. Parameter types include but are not limited to items such as the following: o Time of Day o Date o Character Direction o Monetary Values o Character Shaping o Cursiveness o Weights and Measures o Double Byte Character Set Support The architecture is described in terms of its structural organization and operation. Fig. 1 depicts the structure of the support for the culture specific operations. It is based on the following elements, each of which is described in more detail in subsequent sections. o Culture Specific Exits (CSE) o Culture Specific Tables (CST) o Culture Specific Exit Interface (CSEI) o Element Integration Code (EIC) Culture Specific Exits (CSE) are object or load modules maintained in a library of executable code. Each CSE performs a unique culture specific operation. Operationally they are combined as necessary but functional separation is maintained. Note: The architecture allows for exits to perform other types of operations upon the substitutable parameters such as conversion from one code page and character set to another or table translation of the parameters. - Culture Specific Tables (CST) are used to drive and control the execution of the various CSEs. These tables reside in a source type library such that each member constitutes a table to drive the CSEs for a specific national language. - The tables are designed such that as new parameter types are identified that require CSE support, they can be easily expanded. When the need to implement another national language is required, all that is needed, provided that the necessary CSEs exist, is to build a new CST to drive the invocation of the applicable subset of the set of all CSEs. - The CST consists of an 80 byte character record for each parameter type. The format is self documenting as each record consists of two keyword(value) parameters as shown in Figure ?? on page 26 below. The TYPE keyword identifies the parameter type followed by a predefined encoded value (see "Parameter Typing"). The EXITS keyword identifies one or more CSEs to be invoked, in order, for the specified parameter type. None, one, or multiple exits may apply for any single parameter type. - It is recommended that a naming convention be used for table names that is

to the individual CSEs. It is assumed that the CP/CS for the individual parameters may vary. Normally, one would expect them to be in the base language in which the product was written but this cannot be relied upon in a distributed processing environment. - Note: A variation, provides for the CP/CS of the basic text string to be provided during the initialization phase and retained with the associated CST. In this case, one would be associated with each NLS code provided in the NLS list. This variation is applicable when the text strings come from a single source such as a message file and there is one CP/CS applicable for each national language. - However, in order to provide for the greatest amount of flexibility in the source of the text string, this example of an EIC provides the information on a call by call basis during the operational phase. - The EIC scans the text string from beginning to end searching for the symbolic parameter indicators. They are represented by an '&n' where 'n' represents the position of the parameter in the base language in which the product was written. For example: Text segment &1 text segment &2 text segment &3. = Original text string Text segment &2 text segment &1 text segment &3. = National Language text strin The list of parameters passed to the EIC are in the order in which they would appear in the original text string in the base language, i.e., &1, &2, &3, etc. They may appear in a different order, i.e., &2, &1, &3, etc., in the national language text string. The EIC handles the correlation with possible revised order resulting from translation such that the correct input parameter is inserted into the correct place within the national language text. (The technique used to handle that correlation is not addressed in this design.) When the position of the symbolic parameter within the text string is found, the corresponding parameter from the input parameters is obtained. Based on the parameter type code, the EIC finds the appropriate CST entry and calls, in order, each of the identified CSEs. It is necessary that the routines be called in order. For example, if a date is to be based on a different calendar, the new date should be calculated prior to converting to the format in which the date is to be presented. If it is necessary to call multiple CSEs, the modified parameter from the first becomes the unmodified parameter for the second and so forth. - After all applicable CSEs have been invoked in sequence for a parameter, the EIC replaces the symbolic variable with the final modified parameter, shifting any characters in the basic text string right as necessary. This is done prior to scanning for and processing the next symbolic parameter.

☐ 3. Document ID: NN880556

L5: Entry 3 of 6 File: TDBD May 1, 1988

TDB-ACC-NO: NN880556

DISCLOSURE TITLE: Canonical Representation and Processing Algorithm for Recursive Logic Queries

L5: Entry 3 of 6 File: TDBD May 1, 1988

DOCUMENT-IDENTIFIER: NN880556
TITLE: Canonical Representation and Processing Algorithm for Recursive Logic Queries

Disclosure Text (1):
- A technique is described which uses a canonical representation form, for recursive logic queries, and a processing algorithm that provides efficient processing through

existing relational database optimizers in a loosely-coupled computer system. The canonical form deals with logic queries in function-free "Horn-clause" logic extended for negation. An extended disjuctive normal form (EDNF) representation of logic queries allows efficient processing in loosely coupled environments, but only covers the class of logic queries that are expressed in the function-free "Horn-clause" logic that include recursions involving the queried goal (Query goal). The concept, described herein, presents the canonical form of logic queries that covers most queries in the function-free "Horn-clause" logic extended for negation. The queries include arbitrary recursions, not necessarily involving the Query goal and may involve negations, which cannot normally be expressed in "Horn-clause" logic. Also, the concept provides an extension of relational database languages to include arbitrary recursions. The concept does not cover cases in which negation occurs in a recursion, since this type of query rarely occurs. In the processing of a general recursive query, there are units of information that must be obtained before processing other units; thus there is a partial order in processing these units. Each unit is called a "forest" and is represented in the EDNF. It consists of a set of noncyclic and cyclic trees. A forest must be instantiated before other forests are evaluated. A temporary table is assigned to a forest to ***** SEE ORIGINAL DOCUMENT ***** maintain evaluation results. However, exceptions are provided to handle subqueries, so that a forest can be evaluated, as a subquery, without having to create a temporary table. A forest is formed whenever there is a recursion, which does not involve the Query goal or when there is a negation. In addition, since the result of the Query goal is the answer to be obtained, the Query goal is always designated as a forest. Typically, there is more than one goal in a cycle, and any one of them can represent the forest. A specific goal that represents the forest is defined as the "forest head". Since a forest must be fully evaluated before other forests can be evaluated, there is an inherent partial order in processing the forests. An order between two forests is established if there is a directed path between the two. A forest graph represents this partial ordering, and the evaluation or the query must be done according to this partial order. The concept is illustrated using an example utilizing the following rules: r1: t(X,Y) <-m(X,Y) & *(X,Y) r2: n(X,Y) <-1(X,Z) & q(Z,Y) r3: t(X,Y) <-e(X,Z) & p(Z,Y) r4: p(Z,Y) <-e(Z,L) & p(L,Y) r5: p(Z,Y) <-a(Z,L) & t(L,Y) ***** SEE ORIGINAL DOCUMENT ***** Suppose query ?t(X,5) is issued, then the program graph will appear as shown in Fig. 1. In this case, three forests are needed: one for the Query goal, one for the negated goal, and one for the cycle at P. The EDNF of each forest is shown in Fig. 2. The subscript F denotes that a node is a forest rather than a base table. The algorithm which obtains the EDNF stops expansion if it encounters a forest. This is performed because a forest represents a fully instantiated node. An improvement can be obtained by bypassing forests that are not part of cycles. Also, a forest created due to negation can be bypassed if it is not traversed through the negation edge. For example, the forest p1, as shown in Fig. 2, was obtained by bypassing the forest t1 . Therefore, the partial order among forests t1, n1 and p1 is obtained, as shown in Fig. 3. If a forest does not form a strict partial order and form a cycle among them, it cannot be evaluated independently; instead, all the forests in the cycle must be evaluated iteratively until a fixed point is reached. The set of forests connected by cycles is defined as a "metaforest", usually formed when there are multiple cycles in the program graph that are interconnected with one another. Also, a single forest, not involved in a cycle, is a metaforest. Therefore, a graph of metaforests is truly a tree and represents the partial order of evaluation among metaforests. As in the forest graph, an edge is found between two metaforests, if there is a directional path between the two with the direction of the edge being the same as that of the path. ***** SEE ORIGINAL DOCUMENT ***** An example of a program graph involving multiple interconnected cycles is shown in Fig. 4. It is drawn in a simplified form, where goals t, p and u are chosen as forest heads. The corresponding EDNF of each forest, t1, p1 and u1, is shown in Fig. 5. The forest graph for the program of Fig. 3 is shown in Fig. 6, and the metaforest graph is shown in Fig. 7. Choosing forest heads in a given program graph for optimization is performed so as to reduce the number of forests. An example of choosing forest heads is shown in Fig. 8, where a program graph involves multiple cycles with one node covering all cycles. A simple way of choosing forest heads is to pick t, p and u (one goal node for each cycle) as the forest heads. However, this will create three forest heads, and forests p1F and u1F will form a metaforest for which a fixed point operation is performed. If s is chosen instead of p and u, since s is included in both cycles, one forest head will be sufficient. The resulting forest, the EDNFs for forests t1 and s1, is shown in Fig. 9. ***** SEE ORIGINAL DOCUMENT ***** From this example, the number of forests is minimized by choosing goals that are included in as many cycles as possible, therefore, a set of nodes covers multiple interconnected cycles if each cycle contains at least one node in the set. The objective is to find

the smallest set of nodes that covers the interconnected cycles. The canonical form of a query is a graph of forests, each forest being represented in the EDNF. The following two algorithms are used: a) for constructing the canonical form of a query, and b) for processing the logic query, based on the canonical form: Algorithm for constructing the canonical form Algorithm Canonical(Logic Query) 1. Construct__program__graph 2. Detect__forest__heads 3. For each forest head (FH) do Call EDNF(FH, Forest, Identity__mapping, False,Identity__mapping, FH) 4. Construct the forest graph 5. Construct the metaforest graph Detect__forest__heads: Find the set of forest heads for program graph as follows: 1. For each cluster of cycles interconnected together, find a minimal set of nodes that covers all cycles; designate each node in the set as a forest head. 2. For each negated edge in the program graph, designate the node at the tail side as the forest head. Mark it noncyclic if it is not included in the cycle. 3. Designate Query goal as a forest. Mark it as noncyclic if it is not included in a cycle. Construct__forest__graph: Construct the graph of forests as follows: 1. Create a forest node for each forest head. 2. If there is a directed path between any two forest heads in the program graph, then create a directed edge between them, with the direction of the edge being the same as that of the directed path. Construct__metaforest__graph: Construct the graph of forests as follows: 1. Create a metaforest node for each forest in the forest graph that is not in any cycle. 2. If there is a cluster of interconnected cycles, create a metaforest node that includes all the forests connected by these interconnected cycles. 3. If there is an edge between any two forests in different metaforests, then create a directed edge between them, with the direction of the edge being the same as that of the edge between the two forests. The algorithm EDNF for obtaining an EDNF form of a forest in a general recursive query is described as follows, using the notations: Edgemap: Mapping function described on an edge. The function maps the variable name on the head side of the edge to the variable name on the tail side of the edge. Accmapping: Accumulative mapping function that maps a variable name to another variable name for a unique path between a node and the node where this mapping chin begins. - Accmapping is obtained as a composition of Edgemaps along this path. For example, if variable X in Node 1 was mapped to Y in Node 2, the variable Y in Node 2 to Y in Node 3 and the variable Y in Node 3 to Z in Node 4, then Accmapping(X) = Z at Node 4. - Forest: EDNF for a forest head in consideration. - Origin__forest__head: The head for which the EDNF is being obtained. - This becomes the root of the EDNF. - Node: A node in the program graph Negation: Flag indicating that the edge being traversed is negated. - Algorithm EDNF(Node, Forest, Edgemap, Negation, Accmapping, Origin__forest__head) For every variable (X) in Node newmapping(X) := Edgemap(Accmapping) If node is a goal node Then If Node is a leaf node or (a cyclic forest head but not origin__forest__head) or (a forest head and Negation = true) Then Replace__variable__names Tree =Construct__tree(Node,Origin__forest__head) If Negation = true Then tag Node as a negation node Forest : =Tree Else if Node is Origin__forest__head and this is not the

Disclosure Text (2):
first visit to Origin__forest__head Then Replace__variable__names Tree =Construct__tree(Node,Origin__forest__head) Tag the tree as a cyclic tree Forest :=Tree Else /*nonleaf node or (noncyclic forest head and Negation=false) or Origin__forest__head at the first visit*/ Forest :=they Ù For each child (C) of Node and the corresponding edge (E) If E is negated Then Negationnew :=true Else Negationnew :=false Call EDNF(C,Subforest, EdgemapE, Negationnew, newmapping, Origin__forest__head) Forest : = Forest U Subforest Else If Node is a rule node then Forest:=they Ù For each child (C) and the corresponding edge (E) Call EDNF(C,Subforest, EdgemapE, false, newmapping, Origin__forest__head) Forest := XPROD(Forest, Subforest) END Replace__variable__names: For every variable (X) in the Node, replace X with newmapping 0-1(X). - Construct__tree(Node,Origin__forest__head): Construct the tree having Node as a sole leaf and Origin__forest__head as the root. - XPROD(Forest1, Forest2): construct a set of trees, each tree t ===== being constructed as follows: For each t1 e Forest1 and t2 e Forest2, Leaves(t) :=Leaves(t1) U Leaves(t2) Root(t) := Root(t1) := Root(t2) In addition, if either t1 or t2 (or both) is tagged as a cyclic tree, then t is also tagged as a cyclic tree Note, a set union on Leaves is used because join between two identical nodes with the same binding results in the same node. Algorithm for processing logic queries based on the canonical form Algorithm Eval__Metaforest(Canonical Form Query, Result) 1. Obtain a total order among metaforests according to the partial order specified in the metaforest data structure. - 2. Evaluate each metaforest (MF) according to the total order as follows: If the metaforest contains a single forest(F), Then Eval__forest(F) Else /*the metaforest contains multiple forests*/ Repeat until no change in any forest

For each forest(F) in MF Eval__Forest(F) END Eval__Forest(F): Evaluates the query in EDNF form for a single forest. The result of the evaluation of the metaforest headed by Query goal, the last one in the total order, is the result of the query. The canonical form for efficient processing pertains to a large class of logic queries encompassing most logic queries in function-free "Horn-clause" logic and is extended to include negations. A query can contain arbitrary recursions. The canonical form uses the EDNF as a building block. The EDNF represents a logic query that allows only recursions involving the forest head. It does not allow negation. Consequently, the canonical form solves all the shortcomings of the EDNF. The canonical form provides an advantage in a loosely coupled system, where the database system and the inference engine are independent systems that communicate with each other, such that it does not allow easy creation of temporary tables. This minimization of temporary tables also minimizes the number of joins between temporary tables residing in main memory and database tables on the disk. This significantly reduces the number of calls to the database system.

☐ 4. Document ID: NN8706360

L5: Entry 4 of 6 File: TDBD Jun 1, 1987

TDB-ACC-NO: NN8706360

DISCLOSURE TITLE: Extended Disjunctive Normal Form for Efficient Processing of Re-Cursive Logic Queries

L5: Entry 4 of 6 File: TDBD Jun 1, 1987

DOCUMENT-IDENTIFIER: NN8706360
TITLE: Extended Disjunctive Normal Form for Efficient Processing of Re- Cursive Logic Queries

Disclosure Text (1):
- Described in this article is the Extended Disjunctive Normal Form (EDNF) for efficiently processing a large class of logic queries. This class encompasses all the logic queries in function-free Horn-clause logic having recursions involving the Query goal. EDNF minimizes the need to create temporary tables that contain the intermediate results. It also eliminates the arbitrary processing structure imposed by the user-written rules. This makes it possible for the optimizer to search through alternative query processing strategies and choose the best one. Since the EDNF is in a form most amenable to database query optimization, this technique is especially useful in a loosely-coupled environment in which the existing database system takes care of data retrieval. ***** SEE ORIGINAL DOCUMENT ***** Good performance of inference engines is essential in expert systems that handle large numbers of rules and facts. Function-free Horn- clause logic queries differentiate themselves from conventional database queries in that they allow recursion. Interpretive processing is convenient to handle recursion, but only with sacrifice in performance. Recently, Ullman they*Ù proposed a data structure and algorithm to capture the class of logic queries in Function-free Horn-clause logic. However, the proposed method is inherently inefficient because (1) it requires creation of many temporary tables unnecessarily, and (2) the structure of the query representation (data structure) prohibits optimization of the query. The creation of temporary tables not only wastes CPU and storage resources, but also degrades performance

```
Set     Items   Descript
S1          0   TEFP? OR TEFPFEC OR EXTEND?()FAST()PATH?
S2        859   PERSISTENT? OR RESIDENT? OR "IN"()(MEMOR? OR SRAM OR RAM) -
            OR TSR
S3         12   S2(3N)(TABLE? OR GRAPH? OR CHART? OR TUPL? OR MATRIX? OR M-
            ATRICE?)
S4      64479   SYNTAX? OR FORMAT? OR LANGUAGE? OR SCHEMA? OR SYSTEM?
S5        834   (ACCESS? OR AVAILAB?)(4N)(LIMIT? OR PARAMET? OR OPEN OR CL-
            OSED OR PARTIAL? OR TIER? OR HIERARCH?)
S6          7   S3 AND S4
S7         41   (DROP? OR END? OR KILL? OR STOP?)(3N)(COMMAND? OR SHUTDOWN?
             OR POWERDOWN OR (POWER OR SHUT)()(DOWN OR OFF))
S8          0   S6 AND S5
S9          0   S5 AND S6
S10         1   S3(10N)S4
S11         1   S10 AND (GENERAT? OR CREAT? OR MODIF? OR CHANGE? OR ALTER?
             OR REGENERAT? OR RECREAT? OR AUTHOR)
S12         0   S3 AND S7
S13         0   S3 AND S5
S14        12   S3 NOT PY>1999
S15        12   S14 NOT PD>19990812
File 256:SoftBase:Reviews,Companies&Prods. 82-2002/Aug
         (c)2002 Info.Sources Inc
```

15/3,K/1
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

01710989 DOCUMENT TYPE: Product

PRODUCT NAME: C++ Data Object Library 5.0 (710989)

Code Farms Inc (483583)
7214 Jock Trail
Richmond Hill, ON K0A 2Z0 Canada
TELEPHONE: (613) 838-4829

RECORD TYPE: Directory

CONTACT: Sales Department

REVISION DATE: 001016

...It protects against pointer errors, manages memory, has fewer but smarter classes, makes objects automatically **persistent** , includes **graphs** , ER models, properties and other advanced data structures. The library treats data structures as design...

15/3,K/2
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

01445657 DOCUMENT TYPE: Product

PRODUCT NAME: Geo Whiz (445657)

Appian Logistics Software Inc (548626)
1601 Greenbriar Pl #J
Oklahoma City, OK 73159 United States
TELEPHONE: (405) 692-1683

RECORD TYPE: Directory

CONTACT: Sales Department

REVISION DATE: 991221

...arrows, text, and other graph annotations. Users can also select subsets of their data for **graphing** , for example, all **residents** with a certain income range. Geo Whiz has applications in sales analysis, route planning and...

15/3,K/3
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

01074004 DOCUMENT TYPE: Product

PRODUCT NAME: net.TABLES (074004)

Data Kinetics Ltd (225223)
2460 Lancaster Rd #202
Ottawa, ON K1B 4S5 Canada
TELEPHONE: (613) 523-5500

RECORD TYPE: Directory

CONTACT: Sales Department

REVISION DATE: 020424

Data Kinetics' net. **TABLES** is an **in - memory table** manager for distributed, heterogeneous networks. net.TABLES offers concurrent, reliable network and Internet access. The...

15/3,K/4
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

00118259 DOCUMENT TYPE: Review

PRODUCT NAMES: BroadQuest 2.0 (755842)

TITLE: Portals Made Simple
AUTHOR: Ulfelder, Steve
SOURCE: Computerworld, v33 n29 p73(1) Jul 19, 1999
ISSN: 0010-4841
HOMEPAGE: http://www.computerworld.com

RECORD TYPE: Review
REVIEW TYPE: Product Analysis
GRADE: Product Analysis, No Rating

REVISION DATE: 20020819

...information, has little adverse impact on network performance, according to the vendor. BroadQuest's queried **tables** become memory- **resident** in a dedicated server, so that most requests from users (about 90 percent) are already...

15/3,K/5
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

00098357 DOCUMENT TYPE: Review

PRODUCT NAMES: Oracle 7 7.3 (004233)

TITLE: VLDB Rules...: Newest Oracle Server
AUTHOR: Gill, Philip J
SOURCE: Oracle Magazine, v10 n6 p48(16)(p56(2)) Nov/Dec 1996
ISSN: 1065-3171
HOMEPAGE: http://www.oramag.com

RECORD TYPE: Review
REVIEW TYPE: Product Analysis
GRADE: Product Analysis, No Rating

REVISION DATE: 20010430

...with messaging, collaboration, and directory services. The hash join algorithm enhances complex-query performance using **in - memory** hash **tables** at run-time, to eliminate the need for sorting. Oracle 7 7.3 has a ...

15/3,K/6
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

00088131 DOCUMENT TYPE: Review

PRODUCT NAMES: Oracle 7 7.3 (004233)

TITLE: Oracle7 Release 7.3
AUTHOR: Faris, Steve Mendelson, Neil Sankar, Hari Smith, Gordon Yeniga...

SOURCE: Oracle Magazine v10 n1 p17(2) Jan/Feb 1996
ISSN: 1065-3171
HOMEPAGE: http://www.oramag.com

RECORD TYPE: Review
REVIEW TYPE: Product Analysis
GRADE: Product Analysis, No Rating

REVISION DATE: 20010330

...joins are available in this release to eliminate the need to do sorts through an **in - memory** hash **table** built at run time. Oracle 7 also supports parallel execution of UNION and UNION ALL...

15/3,K/7
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

00083721 DOCUMENT TYPE: Review

PRODUCT NAMES: Sybase System 11 (569241); TopEnd (374431); Tuxedo (276197); Encina Peer-to-Peer Communication Services 2.0 (533297); Open M/SQL (386588)

TITLE: Relational DBs Rev Up for High-End TP
AUTHOR: Francett, Barbara
SOURCE: Software Magazine, v15 n10 p87(5) Oct 1995
ISSN: 0897-8085
HOMEPAGE: http://www.softwaremagazine.com

RECORD TYPE: Review
REVIEW TYPE: Product Analysis
GRADE: Product Analysis, No Rating

REVISION DATE: 19971230

...11 is able to partition and optimize memory for OLTP applications. Users can make critical **tables** memory- **resident** . For larger systems, OLTP requires a three-tier architecture consisting of an application server, database...

15/3,K/8
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

00074779 DOCUMENT TYPE: Review

PRODUCT NAMES: Builder Electronic Buyer's Guide 1994 (551619)

TITLE: An Improvement in Home Improvement
AUTHOR: Staff
SOURCE: CD-ROM Today, v3 n2 p22(2) Feb 1995
ISSN: 1069-4099

RECORD TYPE: Review
REVIEW TYPE: Review
GRADE: A

REVISION DATE: 20010430

...speeds up building-supplies comparison, providing information from 1,700 manufacturers who make 5,200 **residential** fixtures. **Graphics** , text, and video enliven views of plumbing fixtures, paints, and countertops, only a few of...

15/3,K/9
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

00074349 DOCUMENT TYPE: Review

PRODUCT NAMES: Visual FoxPro 3.0 (546135)

TITLE: Visual FoxPro 3.0: First Look
AUTHOR: Koorhan, Leslie
SOURCE: Data Based Advisor, v13 n2 p50(4) Feb 1995
ISSN: 0740-5200
HOMEPAGE: http://www.advisor.com

RECORD TYPE: Review
REVIEW TYPE: Product Analysis
GRADE: Product Analysis, No Rating

REVISION DATE: 19990730

...environment supports events, methods, and properties. Database containers are now available, to let developers establish **persistent** relationships between **tables** . The Project Manager has been improved, and users are now presented with convenient tabs for...

15/3,K/10
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

00074047 DOCUMENT TYPE: Review

PRODUCT NAMES: Visual FoxPro Windows (546135)

TITLE: FoxPro moves to objects
AUTHOR: Zimmelman, Steve
SOURCE: InfoWorld, v17 n4 p1(2) Jan 23, 1995
ISSN: 0199-6649
HOMEPAGE: http://www.infoworld.com

RECORD TYPE: Review
REVIEW TYPE: Review
GRADE: A

REVISION DATE: 20020228

...precision floating-point number, Currency, and DateTime. It is very easy and visual to establish **persistent** relationships between database **tables** ; with a simple point and click, the relationship is stored in the data dictionary. Windows...

15/3,K/11
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

00070754 DOCUMENT TYPE: Review

PRODUCT NAMES: RenderPrint 1.1 (532398)

TITLE: RenderPrint v1.1
AUTHOR: Liddle, Art
SOURCE: CADalyst, v11 n10 p32(1) Oct 1994
ISSN: 0820-5450
HOMEPAGE: http://www.cadonline.com

RECORD TYPE: Review
REVIEW TYPE: Review

GRADE: A

REVISION DATE: 19990530

...is easy to configure, and its current settings govern printing. Users can print from any **graphics** application through a **TSR** version. Multiple image files can be processed with a batch mode. The print preview option...

15/3,K/12
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

00060919 DOCUMENT TYPE: Review

PRODUCT NAMES: Microsoft SQL Server Windows NT (259748)

TITLE: SQL Server for Windows NT
AUTHOR: Roti, Steve
SOURCE: DBMS, v7 n1 p97(2) Jan 1994
ISSN: 1041-5173
HOMEPAGE: http://www.dbmsmag.com

RECORD TYPE: Review
REVIEW TYPE: Product Analysis
GRADE: Product Analysis, No Rating

REVISION DATE: 20000830

...administration enhancement is the ability to place the Tempdb database, a storage space for temporary **tables** , **in memory** , rather than on disk. This can help speed up operations, but may make less memory..

```
Set     Items   Descript[redacted]
S1         21   TEFP? OR [redacted]PFEC OR EXTEND?()FAST()PATH?
S2    1469172   PERSISTENT? OR RESIDENT? OR "IN"()(MEMOR? OR SRAM OR RAM) -
             OR TSR
S3       6044   S2(3N)(TABLE? OR GRAPH? OR CHART? OR TUPL? OR MATRIX? OR M-
             ATRICE?)
S4   12809835   SYNTAX? OR FORMAT? OR LANGUAGE? OR SCHEMA? OR SYSTEM?
S5     302447   (ACCESS? OR AVAILAB?)(4N)(LIMIT? OR PARAMET? OR OPEN OR CL-
             OSED OR PARTIAL? OR TIER? OR HIERARCH?)
S6       3663   S3 AND S4
S7      15391   (DROP? OR END? OR KILL? OR STOP?)(3N)(COMMAND? OR SHUTDOWN?
              OR POWERDOWN OR (POWER OR SHUT)()(DOWN OR OFF))
S8          0   S3(5N)S4(5N)S5
S9         13   S3(S)S4(S)S5
S10        22   S3 AND S4 AND S7
S11         0   S S3(4N)(CREAT? OR AUTHOR? OR MODIF? OR CHANG? OR EDIT? OR
             RECREAT? OR GENERAT? OR REGENERAT?)
S12      1037   S3(S)(CREAT? OR AUTHOR? OR MODIF? OR CHANG? OR EDIT? OR RE-
             CREAT? OR GENERAT? OR REGENERAT?)
S13       266   S12(S)S4
S14        14   S12(S)S5
S15         1   S12(S)S7
S16        96   S12(5N)S4
S17        67   S3(10N)(CREAT? OR AUTHOR? OR MODIF? OR CHANG? OR EDIT? OR -
             RECREAT? OR GENERAT? OR REGENERAT?)(5N)S4
S18        45   S9 OR S10 OR S14 OR S15
S19        33   RD (unique items)
S20        31   S19 NOT PY>1999
S21        31   S20 NOT PD>19990812
File 275:Gale Group Computer DB(TM) 1983-2002/Sep 26
         (c) 2002 The Gale Group
File  47:Gale Group Magazine DB(TM) 1959-2002/Sep 25
         (c) 2002 The Gale group
File 636:Gale Group Newsletter DB(TM) 1987-2002/Sep 26
         (c) 2002 The Gale Group
File  16:Gale Group PROMT(R) 1990-2002/Sep 26
         (c) 2002 The Gale Group
File 624:McGraw-Hill Publications 1985-2002/Sep 25
         (c) 2002 McGraw-Hill Co., Inc
File 484:Periodical Abs Plustext 1986-2002/Sep W4
         (c) 2002 ProQuest
File 613:PR Newswire 1999-2002/Sep 26
         (c) 2002 PR Newswire Association Inc
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 621:Gale Group New Prod.Annou.(R) 1985-2002/Sep 25
         (c) 2002 The Gale Group
File 674:Computer News Fulltext 1989-2002/Sep W4
         (c) 2002 IDG Communications
File  15:ABI/Inform(R) 1971-2002/Sep 26
         (c) 2002 ProQuest Info&Learning
File   9:Business & Industry(R) Jul/1994-2002/Sep 25
         (c) 2002 Resp. DB Svcs.
File 647:CMP  Computer Fulltext 1988-2002/Sep W2
         (c) 2002 CMP Media, LLC
File 148:Gale Group Trade & Industry DB 1976-2002/Sep 26
         (c)2002 The Gale Group
File 634:San Jose Mercury  Jun 1985-2002/Sep 25
         (c) 2002 San Jose Mercury News
```

21/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02116411 SUPPLIER NUMBER: 19952429 (USE FORMAT 7 OR 9 FOR FULL TEXT)
ANGARA DOES HIGH-SPEED DISKLESS DATABASE-IN-RAM.
Computergram International, n3283, pCGN11050003
Nov 5, 1997
ISSN: 0268-716X LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 368 LINE COUNT: 00031

TEXT:
Stanford University spin-out Angara Database **Systems** Inc has taken Oracle Corp's VLM database-in-RAM concept to its logical conclusion...

...5m venture funding from Kleiner Perkins Caufield & Byers and will make its Main Memory Database **available** on a **limited** basis in December. It's designed to provide high- speed analysis of complex data sets typically 500Mb to 2Gb in size and is claimed to handle the permanently memory **resident tables** ten times faster than the cache of a standard disk-based database. Key difference between...

21/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01804821 SUPPLIER NUMBER: 17155728 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Client/server and host app. development tools. (1995 Database Buyer's Guide and Client/Server Sourcebook) (Buyers Guide)
DBMS, v8, n6, p20(13)
May 15, 1995
DOCUMENT TYPE: Buyers Guide ISSN: 1041-5173 LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 20277 LINE COUNT: 01789

... Mountain View, CA
415-321-2238; 600-876-4900
Offers the following components, which are **available** separately: **Open** Interface Elements 3.0 (GUI), C/S Elements 1.5 (GUI and data access); Smart...

...intuitive. The business rule module enables users to add simple or complex business rules to **create** smart applications. Provides a visual point-and-click development environment that includes four facilities that integrate the components into a development environment: a scripting **language** ; visual **editors** ; C and C++ support; and numerous portable application services such as **graphic** primitives, built- **in memory** , error handling, file I/O, and string manipulation services. Prices start at $6500 (no runtime...

21/3,K/3 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01765504 SUPPLIER NUMBER: 16704858 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Visual FoxPro 3.0: first look. (Microsoft's database development software) (Software Review) (Evaluation)
Koorhan, Leslie
Data Based Advisor, v13, n2, p50(4)
Feb, 1995
DOCUMENT TYPE: Evaluation ISSN: 0740-5200 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2556 LINE COUNT: 00191

...ABSTRACT: easier. The product offers object-oriented capabilities and database containers that allow for implementation of **persistent**

relationships between **tables** . The new version provides the latest in OLE including OLE controls and the ability to...
... more to VFP than just OO. You now get database containers so you can establish **persistent** relationships between **tables** . You also get validations and triggers that can be stored in the database, rather than... event in a command button, then you can trigger the code by using the same **syntax** , MyButton.Click. Visual FoxPro lets developers create their own properties and methods, which can be...ll find many of these commands relatively easy to understand since they follow the FoxPro **format** . For example, you have DEFINE CLASS and **END** DEFINE **commands** , and a CREATEOBJECT() function. There are many more for this topic and this ability in Visual FoxPro conforms to the major definitions of an object-oriented programming **language** . You'll find that VFP supports encapsulation, inheritance, and polymorphism.
Using object orientation, you'll...

...starts the process, allowing us more modeless forms and menus than before, and the second **command** **ends** the event process. No more Foundation READ, and no more event handler code to maintain...

21/3,K/4 (Item 4 from file: 275)

01463405 SUPPLIER NUMBER: 11590096 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Anti-virus programs. (includes related article on Viruses used in testing) (Software Review) (Evaluation)
PC User, n172, p150(10)
Nov 20, 1991
DOCUMENT TYPE: Evaluation ISSN: 0263-5720 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 6548 LINE COUNT: 00570

... OSPL Compusec
* Tel (0252) 812112 Fax (0252) 812819
* Availability Now
* Price See table
* Updates See **table**
Strengths
* **TSR** causes minimal delay
* Password file protection
* Password protects configuration files
Weaknesses
* Slow scanning
* Poor manuals...
...and scope of their replication. Networking, computer mail, bulletin boards and sharing software all leave **systems** open to virus infection and replication. Standardised procedures can reduce the chance of an infection ...

...or prepend themselves to an executable file, most commonly files with COM or EXE extensions. **System** viruses infect specific **system** files such as COMMAND.COM.
File and **system** viruses use two different approaches in attacking other files. Some viruses scan the DOS directory...

...programs.
Stealth viruses such as 4096 (Frodo) evade detection in some cases by returning infected **system** components to their normal, uninfected state whenever they're read and reinfecting the **system** after the read operation is completed. Another stealth technique is to encrypt code differently for ...and a module that incorporates security features not found in any other programs. It controls **system** access rather than merely preventing access. Virus Prevention Plus demonstrates strength in **system** security.
The boot track is encrypted and almost tamper-proof, but an anti-virus program...
...retrieving data from the hard disk). The program focuses on corporate

use and protection of **systems** with sensitive data or handling vulnerable operations. The interface can be daunting, and installation intimidating... checks the programs' prevention of attempts to modify the boot sector and partition table and **format** the disk.

The overall quality scare is a weighted average of scores for the individual...

...protection options for the entire disk, executable files and the boot sector, and it prevents **formatting** of the disk, warns of direct disk writes and identifies TSR programs.

Novi, Certus 2...hard drive, Microsoft serial mouse and NEC MultiSync 2A VGA monitor.

The hard drive is **formatted** before each test program is run and Lotus 1-2-3 Release 2.3, Microsoft...

...10).

The auto-timing batch file uses Norton Control Centre with the /start:n and / **stop** :n **commands** . A set of eight commands checks the delays imposed on invoking programs (Mode, Append, Print, **Format** , Chkdsk, Xcopy, Recover and Cls).

Quality

Quality evaluations assess each program's ability to catch...

...through attempts to overwrite the boot sector, changing the header in an executable file and **formatting** the disk.

A. Scanning

...well as macros, can also be altered to include viruses.

Once installed on a freshly **formatted** drive with 455 files, the TSR portion of the program is invoked. The program scans all the executable files and **system** memory, and the benchmark is repeated with memory checking disabled.

Analysis

The programs' scanning times...an executable fine and the boot sector. The remaining test consists of an attempt to **format** the hard disk and change the partition table.

Analysis

Novi and Virex-PC excel at...

...infect files. Novi permits Fish, Dot Killer and Sverdlov to infect files. It cleans Dot **Killer** from **COMMAND** .COM on reboot, but Sverdlov and Noviboot (Novi's boot protection module) alternatively infect and clean, causing the **system** to keep rebooting. Like Certus 2.1, Novi can set the DOS attribute to read...

...OF LOGIC BOMBS

Conditions	Harmful Activity
Certain date	Delete files
Certain day (eg. Friday 13th)	**Format** the hard disk
Specific number of reboots	Cross-links files
Specific number of infections	Change...Cascade (1701).

Fish (Fish6)

Infects all executable files, but immediately goes for COMMAND.COM. Infects **systems** running DOS 3.0 or later. Stores, changes and restores file attributes, hides the change...

...example of a stealth virus. The virus spends so much time hiding, it slows the **system** to the point of detection.

Dot Killer

Infects COM files, including COMMAND.COM.

Ita Vir...

...DESCRIPTORS: **Systems** /Data Security Software

...TRADE NAMES: Norton AntiVirus (**Systems** /data security software...

21/3,K/5 (Item 5 from file: 275)

01452322 SUPPLIER NUMBER: 11378405 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Designing Paradox network applications. (tutorial)
Rowe, Robin
TECH Specialist, v2, n9, p21(6)
Sept, 1991
DOCUMENT TYPE: tutorial ISSN: 1049-913X LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 3857 LINE COUNT: 00289

ABSTRACT: Paradox, a relational data base management **system** (DBMS) from Borland International, can be used to design applications programs for networks. The programmer...

...be added to one another, emptied, deleted, copied, sorted, queried and designed. Because Paradox Application **Language** (PAL) is a macro **language** , programmers must be acquainted with Paradox in the interactive environment.
... indices, and image settings, belong to a table and are called its family.
Paradox Application **Language** (PAL) is a macro **language** , so you must be intimately acquainted with Paradox in the interactive environment to get anywhere...requests. An unposted record by a user away from their terminal can lock up a **system** indefinitely, so network PAL programmers try to issue UNLOCKRECORD soon after a WAIT TABLE. You...

...Paradox application. To do this, access reports through the menus instead of using the REPORT **command** . Unfortunately, you cannot **stop** a runaway query.
Form And Link Locks
Paradox enforces referential integrity through its forms. You... fields. Wide tables incur a performance penalty. A table with 255 fields will grind your **system** to a halt. Circumstances vary, but start looking for ways to split a table when...

...not the best way to pack it. During a restructure, Paradox holds part of the **table in memory** only. A power interruption at the wrong moment will irrevocably destroy the table. The best...error handler allows the user to recover automatically from most errors, or shut down the **system** in an orderly way. Without an errorproc, the user faces the Cancel/Debug prompt in...

...directly into Paradox. Paradox imports and exports dbase, 1-2-3 and several other file **formats** directly. To export fixed length fields, simply create a one-line report.
The included Personal...

...need DesqView or Windows. Paradox works well under DesqView, but you must mark the Paradox **system** files as read-only during configuration. You have to run Paradox in real mode under...

...to struct tables, and translating a remote Query By Example (QBE) into a Structured Query **Language** SQL) server request. Each user connected on SQL Link requires two network user counts, since...

DESCRIPTORS: Relational Data Base Management **Systems** ;

21/3,K/6 (Item 6 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01440576 SUPPLIER NUMBER: 11005248 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Microsoft Works. (Microsoft Corp.) (Software Review) (one of nine evaluations of integrated software packages in 'Integrated Software Under $200.') (evaluation)
Perratore, Ed
PC Magazine, v10, n14, p283(3)
August, 1991

DOCUMENT TYPE: evaluatio[redacted] ISSN: 0888-8507 LANGU[redacted] ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 984 LINE COUNT: 00076

... and variable line spacing within one document.
You can also block text for further action, **limited** only by **available** RAM. Data transfer from one application to another is usually as simple as selecting, copying, switching, and pasting. Inserting a graph requires only that the spreadsheet whose data you have **graphed** is active **in memory** at the same time. Once you insert the appropriate merge command into the document, you can adjust the graph's height, **change** its orientation, position it horizontally or vertically, and view it on-screen before printing.
There...

21/3,K/7 (Item 7 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01380378 SUPPLIER NUMBER: 09597763 (USE FORMAT 7 OR 9 FOR FULL TEXT)
An object-oriented relational database. (Computing Practices)
Premeriani, William J.; Blaha, Michael R.; Rumbaugh, James E.; Varwig, Thomas A.
Communications of the ACM, v33, n11, p99(11)
Nov, 1990
ISSN: 0001-0782 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 7001 LINE COUNT: 00573

...ABSTRACT: data models also avoid normalization problems that can occur with relational database design. OO programming **languages** (OOPL) improve modularity, code reuse and code maintenance. A technique for constructing an object-oriented database management **system** (OO-DBMS) is to buffer the database with an object-oriented layer that retains relevant...
Many people recognize the short-comings of current database management **systems** (DBMS) [2, 9, 10] and conventional programming **language** [4, 8]. DBMS and programming **languages** each provide a distinct viewpoint on data and applications. The two viewpoints are not well...

...needed for advanced applications, such as abstract data types, complex integrity constraints, and versioning. Programming **languages** , such as Pascal and C++, provide abstract data types, structured control constructs, and the ability...

...applications and avoid the normalization problems often associated with relational database design [3]. OO programming **languages** (OOLPs) improve code reuse, code maintenance, and modularity [8].
We describe a technique for constructing...

...applications are unaware that they are receiving DBMS services. The programmer sees an object-oriented **language** with certain predefined operations that allows objects to be retrieved from and stored in a...

...OOPL into a robust and efficient OO-DBMS. Our OO-DBMS is not a complete **system** . It lacks commonly expected features such as extensible data types, management of behavior as well...
...the most important features of an OO-DBMS is the implicit assumptions that (1) the **system** is oriented toward operations on individual objects and (2) the programmer can expect these to...

...two basic approaches to OO-DBMS: extending a relational DBMS and extending an OO programming **language** .
One can implement an OO-DBMS by extending an RDBMS. One extends the relational model...

...approach combines the maturity and robustness of the RDBMS with the performance of the OO **language** in an open architecture that makes it convenient to interface with other **languages** . Also, you can have both an

OO and a relational inte[redacted]ce to the same database...

...important for the success of the shadowing technique, which we use to interface the programming **language** to the database.

Object-Oriented Modeling

We have been using the Object Modeling Technique (OMT...Relational DBMS (RDBMS)

The RDBMS must provide that persistence, concurrency control, transactions, and a programming **language** interface. A query **language** or query-by-forms capability is unimportant for many engineering analysis problems because access to...

...be regarded as a lower-level resource invisible to the end user.

Object-Oriented Programming

Language (OOPL)

The object-oriented programming **language** must provide objects of different classes and the ability to send messages to objects to...

...Inheritance of methods is not required by the algorithm presented here, although any reasonable OO **language** will have it. Each class describes a set of objects with identical structure. A class...

...RDBMS tables. The other relationship are stored in object tables as buried pointers.

OO-DBMS **System**

Architecture

The programmer views the OO-DBMS as an object-oriented **language** with persistence. The **language** includes specific operations about instances of classes and relationships. The OO-DBMS has both compile...

...on by a conversion process. The conversion output is a run-time programming interface (OO **language** subroutines and DDL commands to generate RDBMS tables.

Initially the conversion process was partially automated...

...a general purpose graphics editor. The graphics editor produces graphics output in an ASCII markup **language** for which we have a BNF description. We used LEX and YACC (2) to compile...

...section on OO-DBMS Programming Interface, later). These routines access buffered objects through an OO **language** . The shadowing routines access the relational database through the RDBMS programming interface (usually cursors on...

...criterion for the OO-DBMS. The shadowing mechanism improves interactive performance by using the OO **language** to search memory and by deferring database writes. Most read operations can be performed without...a database. To a large extent the programmer can think in terms of the OO **language** and forget about database interface details. OO **languages** also provide robust libraries of tested code and facilitate code reuse.

The OO-DBMS reduces programming errors since the programmer does not ecome confused by the mismatch between programming **languages** and data-base **languages** . Instead of using linked lists, trees, and hash tables, one operates on objects and relationships...

...is accessed directly from the database and locked for the shortest possible amount of time. **System** data for section (discussed later) is an example of concurrent data. In contrast, buffered data...

...look alike to the programmer; both categories support the same operations and have the same **syntax** . The OO-DBMS keeps track of which objects are buffered and which are concurrent. The only difference between the two categories is the time at which **changes** are committed to the database and the degree of concurrency. Updates on concurrent tables are immediately applied to the database. Updates on buffered **tables** are accumulated **in** **memory** for later writing upon an explicit save **command** or at the **end** of a session. In practice, only a few tables contain data that must be share...

...OO-DBMS: database or [redacted]database. Database classes and [redacted]lationships are handled both by the OO **language** and the RDBMS and may be saved in the database. Nondatabase definitions are handled only by the OO **language** and may not be saved. Both kinds are useful. There is no point in creating...

...from participating objects as the primary key.

All IDs are 32 bits long because the **system** is being run on a 32-bit machine. Section IDs use only 16 bits and...new empty transient object of the given class. Issues a create request to the buffering **system** . After an object is created, data may be entered with a PUT operation. An object...

...Fills in an attribute by overwriting previous contents. Issues an update request to the buffering **system** .

GET (attributename, object)

Returns an attribute value from an object. No action is required by the buffering **system** .

RETRIEVE (classname, keyname, value 1, . . .)

Returns a set of persistent objects whose keys match the...

...Converts a transient object into a persistent one. Issues an insert request to the buffering **system** . An error is raised if the object violates database integrity.

DELETE (object)

Destroys an object. Issues a delete request to the buffering **system** . An error is raised if the object belongs to any relationship.

COPY (object)

Returns a transient copy of the object, including its data. Issues a create request to the buffering **system** . COPY is equivalent to NEW followed by many GETs and PUTs.

Operations on Relationships

The...

...a pair of persistent objects to a relationship. Issues an insert request to the buffering **system** .

DELETE (relationshipname, obj 1, obj2)

Deletes an object pair from a relationship. Issues a delete request a delete request to the buffering **system** .

DELETE-1 (relationshipname, obj1)

Deletes all object pairs from a relationship where obj1 is the first object in the pair. Issues a delete request to the buffering **system** for each pair.

DELETE-2 (relationshipname, obj2)

Deletes all object pairs from a relationship where obj2 is the second object in the pair. Issues a delete request to the buffering **system** for each pair.

RETRIEVE-1 (relationshipname, obj1)

Searches relationship to find object pairs in which...

...changes for a given section to the database. Save requests are issued to the buffering **system** for objects and relationships requiring insertion, deletion, or updating.

Internal Buffering

Mechanism

The programmer accesses...

...DELETE. An insert from this state is an error.

Internal Buffering Operations

The database buffering **system** is driven by ...deferred insertion followed by a deferred deletion cancels out, leaving no trace in the buffering **system** .)

(3) Deletions must be processed before insertions, in case there is a duplicate record with...

...Linkage

The OO-DBMS must quickly map from the database primary key to the OO **language** pointer and vice versa. Some possible implementation techniques are:

(1) pair of tables hashing
(2) pair of trees.

We used the container class relationship of our OO **language** , which was implemented with a pair of tables plus hashing. Hashing algorithms and table lookup are provided by OO **language** libraries.

Integrity Checking

The OO-DBMS incorporates rudimentary integrity checking. The OO-DBMS enforces the...

...RDBMS by rewriting the database interface. The OO-DBMS could be ported to another OO **language** by emulating the DSM relation feature [19].

We chose the MIMER[R] DBMS for reasons...

...cannot be composite.

We chose the Data Structure Manager (DSM) [19, 22] as our OO **language** because of its technical features and in-house availability. DSM is a full-functionality OO **language** developed at GE. DSM runs on top of the C **language** . The most noteworthy DSM feature is its support for relationships among objects. One can navigate...

...can take an existing relational DBMS (RDBMS) and hide it beneath an object-oriented programming **language** . The buffering algorithm yields fast interactive performance while storing objects in a database. Our work...

...get good performance.

This approach combines the best features of both RDBMS and OO programming **languages** . RDBMSs have a sound theoretical base and work well for business applications. Commercial products have...
...same time we obtain the benefits of using objects to abstract an application. The programming **language** allows complex algorithms to be written that would be hard to express in an RDBMS...

...subsystems. An OO design methodology is the "glue" that binds together the RDBMS and OO **language** . Our "OO-DBMS" lacks the functionality of a full **system** . Nevertheless, our approach to an OO-DBMS is quite effective for many applications.

In our applications, we have found that OO programming improves programmer productivity, relative to conventional procedural **languages** like Pascal and C. Our approach to an OO-DBMS enables one to reap these...

...2) LEX and YACC are Unix tools.

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...Engineering]: Design--methodologies; H.2.1 [Database Management]: Logical Design; H.2.4 [Database Management]: **Systems**
General Terms: Design, Performance
Additional Key Words and Phrases: Database checkout, database performance, database shadowing...

...and is working on object-oriented methodologies for software design and their implementation as practical **systems** for applications. Email: rumbaugh[a]crd.ge.com
THOMAS A. VARWIG is a senior software...

21/3,K/8 (Item 8 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01354498 SUPPLIER NUMBER: 08284734 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Good form. (Orbit Enterprises' Formset forms development software) (Software Review) (evaluation)
Pereira, David A.
Data Based Advisor, v8, n4, p20(1)
April, 1990
DOCUMENT TYPE: evaluation ISSN: 0740-5200 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 529 LINE COUNT: 00040

...ABSTRACT: available from Orbit Enterprises Inc for $189.95. It works with dBASE applications and other **languages** to generate forms, but for laser printers only. With Formset, the designer creates the form...

...cautious with file names because Formset uses the extension 'frm' as does dBASE, but the **format** of the files is different. Formset requires only command **syntax** and does not have a forms design interface using WYSIWYG. The documentation and the samples...
... Orbit Enterprises, Formset is a forms generator that works with dBASE applications (or any other **language** for that matter). Formset has a programming **language** that's compiled into the LaserJet's Printer Control **Language** (PCL) and copied into your LaserJet's memory. Formset only works with laser printers.
Let...

...DOS to copy the entire file and ignore any end-of-file markers.
Formset offers **endless** power. Its drawing **commands** are extensive. It can incorporate a variety of shaded areas, line drawings, **resident** or cartridge fonts, **graphic** images, and extensive error checking and reporting.
So, what's wrong with Formset? Not much...

...t have an on-screen forms designer interface using WYSIWYG; it only uses a command **syntax** . This won't pose a problem if you program in dBASE--the

Formset **language** is fa[redacted]y simple. Finally, while compi[redacted]g, Formset displays the form on the screen in preview...

...than outstanding. It's easy to use and powerful if you develop applications. The command **syntax** is very simple to master. On-disk examples and the manual will get you creating...

21/3,K/9 (Item 9 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01301390 SUPPLIER NUMBER: 07397328 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Videoscope: a nonintrusive test tool for personal computers. (includes related article on video signature analyzer operation) (technical)
Tuttle, Myron R.; Low, Danny
Hewlett-Packard Journal, v40, n3, p58(7)
June, 1989
DOCUMENT TYPE: technical ISSN: 0018-1153 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 4580 LINE COUNT: 00350

ABSTRACT: Hewlett-Packard's Videoscope **system** performs nonintrusive, automated performance, compatibility and regression testing of applications running on the company's HP Vectra Personal Computers. The user enters test data manually, but the Videoscope **system** automatically executes the application that uses the data, uses signature analysis techniques to test the application and displays and records the results. The Videoscope **system** consists of the 'vscope' program which is used to create and execute the tests and the Videoscope board which links the host **system** to the **system** under test. Details of the design and functioning of the software and board are described. The Videoscope **system** is not available as a product.

INTERACTIVE TESTING OF APPLICATION SOFTWARE requires the tester to sit at the test **system** and enter test data using a keyboard and/or some other input device such as...

...of interactive applications running on HP Vectra Personal Computers. It is independent of the operating **system** and nonintrusive. Nonintrusive means that it does not interfere with or affect the performance and behavior of the application being tested or the operating **system** . Videoscope is for internal use and is not available as a product.

An overview of...

...screen displays. These tools and certain standards for creating tests were called the regression test **system** (RTS).

While RTS initially proved adequate, long-term use revealed weaknesses in the **system** . First, mouse movements could not be captured or played back, so any program that used a mouse had to be tested by hand. Second, the **system** was intrusive. This meant that certain programs did not act the same when RTS was...

...the application. Finally, RTS could not be used to do performance testing since it used **system** resources and affected the performance of the **system** .

Videoscope was developed to replace RTS and to compensate for its weaknesses. This resulted in the following design objectives for the Videoscope **system** :

* It had to have the same capabilities as RTS.
* It had to be nonintrusive.
* It...

...are inserted in the test scripts to control when certain events take place on the **system** under test. Real-time performance testing means the ability to determine the actual response time of events taking place on the **system** under test.

* It had to be able to handle a mouse and any other pointing...

...of this objective is [redacted]e able to port test scripts t[redacted]her PC operating **systems** such as Xenix, OS/2, or even HP-UX. It was also considered necessary to be able to use a multitasking computer **system** such as the HP 3000 Computer **System** as a host to test multiple **systems** on playback.

* It had to be able to handle a list of programs (e.g...

...HP AdvanceWrite) that we needed to test but were unable to test with RTS.

Videoscope **System**

The Videoscope **system** consists of two major parts: a program called vscope that resides in a **system** known as the host **system** , and a board called the Videoscope board that occupies one slot in the PC running the application being tested (see Fig. 2). This **system** is called the **system** under test (SUT). The vscope program is used by the tester to create and perform...need to look at it. Also for playback, it is possible to use any computer **system** with appropriate software as the host--not just a PC. This satisfies the portability objective...

...provides the interface between the tester and the recording and playback features of the Videoscope **system** . For recording the tester uses the keyboard and pointing device on the host and runs...

...most frequent ones are included in a signature list, which goes into the file.

The **syntax** of the symbolic names and the algorithm to interpret them is based on those commonly...

...w [cmd]getcrc[cmd] results in a clear screen, a listing of filenames in wide **format** on the SUT, and the capture of the resulting screen in the signature file. These...
...cause distruption on the host.

The pattern [cmd] is used to mark the beginning and **end** of a vscope **command** . Some vscope commands translate directly into commands used by the Videoscope board firmware, and other...

...other hand, the vscope log command, which writes information to a file on the host **system** , has no association with the Videoscope board. Other commands translate into a complex series of...mode called the replay or regeneration mode. Screen signatures are highly dependent on the video **system** in use. Even though the display may look exactly the same, signatures from an HP...

...Board

The Videoscope board is partitioned into two major sections: the Videoscope processor and the **system** under test interface (see Fig. 5). The two sections operate independently and are connected by...

...low cost and high level of integration, and the fact that it used the same **language** development tools as the Intel 80286. The 80188 contains built-in timers, DMA controllers, an...

...need for at least two 40-pin packages and several smaller-scale chips.

The processor **system** is equipped with 32K bytes of ROM and 8K bytes of RAM. Connected as peripheral...

...the HP-HIL protocol.

The Videoscope processor firmware is written entirely in Intel 80188 assembly **language** . It is modular and all main routines are reached through a jump **table in RAM** . A loader function is provided so that a user can write a custom module and...

...entry to a user module. The firmware is structured as a real-time interrupt-driven **system** . The code normally sits in an idle loop until a command needs to be processed...

...processing routines themselves introduce new interrupt service routines for their operation.

Communication with [redacted] host **system** is through the [redacted]-232-D interface shown in Fig 5. The firmware supports up...successful completion the field may contain actual data. If it does, it is in a **format** similar to a command, including a length and a checksum. In the case of a...to avoid conflicts with hardware installed in the SUT. The current implementation of the Videoscope **system** does not make use of the SUT interface. However, the hooks are available for users...
...purpose testing requirements.

Conclusion

Videoscope has met or exceeded the original objectives established for the **system** . One minor disappointment is that the the signature generated from the video signal is not...

...productivity tool to improve the quality of software. The PC intrinsically is an interactive computer **system** . This means that batch-style tests cannot adequately test the capability of any software written...

...alternative to slow, error-prone, and expensive manual testing. Currently there are over 100 Videoscope **systems** in use at 18 HP divisions.

Acknowledgments

We would like to acknowledge the help of...
CAPTIONS: An overview of the operation of the Videoscope **system** . (chart) ; Typical setup for using the Videoscope **system** with an HP Vectra PC. (chart); Data flow during test script recording. (chart)

21/3,K/10 (Item 10 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01213340 SUPPLIER NUMBER: 05158766 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Get the full EGA color spectrum. (producing a custom color palette for enhanced graphics adapters using SPECTRUM software) (PC Lab Notes) (column)
Hummel, Robert L.
PC Magazine, v6, n12, p311(14)
June 23, 1987
DOCUMENT TYPE: column ISSN: 0888-8507 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 6760 LINE COUNT: 00509

... in the EGA ROM BIOS and shown in Table E. The EGA BIOS provides for **changing** these values (as well as other **parameters**) by **accessing** them through a pointer. Our programs can **create** a new **table in memory** and, by aiming pointer at them, cause our parameters to become the default. The process...

...the way memory-resident programs attach themselves to interrupts the palette registers can also be **changed** individually through a BIOS call or by programming the Attribute Controller.

The EGA can produce...

21/3,K/11 (Item 11 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01208784 SUPPLIER NUMBER: 06077704 (USE FORMAT 7 OR 9 FOR FULL TEXT)
How protected mode protects.
Mirecki, Ted
PC Tech Journal, v5, n11, p80(4)
Nov, 1987
ISSN: 0738-0194 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2115 LINE COUNT: 00160

... interlevel control transfers. One type of control descriptor is

described later in this [redacted]ebar.
Descriptor **tables** are built **in** **memory** , but memory cannot be accessed until descriptor tables are built. In order to break this chicken-and-egg impasse, the GDT is created by the operating **system** before the switch to protected mode, when the lower 1MB of memory is directly accessible...

...are created in protected mode, in memory defined by descriptors in the GDT. The operating **system** builds an LDT for a task at load time, creating an initial set of descriptors...

...LDT are created and destroyed in response to memory-allocation requests from the task. All **access** to descriptor tables is **limited** to code executing at privilege-level zero.
Protection checks are applied by the hardware at...

21/3,K/12 (Item 12 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01207893 SUPPLIER NUMBER: 04644240 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Ventura Publisher: beauty and brains. (Software Review) (evaluation)
Burns, Diane; Venit, S.
PC Magazine, v6, n3, p150(5)
Feb 10, 1987
DOCUMENT TYPE: evaluation ISSN: 0888-8507 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 5498 LINE COUNT: 00425

...ABSTRACT: documents. Style sheets are included in the program, so that user's can delineate the **format** and the font of repeating elements such as major headings or body text. The user...
... compromises (see sample).
Ventura incorporates style sheets that let you define the font and the **format** of repeating elements such as body text and major heading. You can change the **format** of an entire document by simply modifying the style sheet (a feature of many word...

...be isolated in widows or orphans. It lets you import text in six different file **formats** , and edits made later in the source file will be reflected in the Ventura Publisher...

...placed. The tag mode is used for assigning tags to text, as well as for **formatting** the style attributes of each tag. The text mode is used when editing text or...

...of pages you can create in one file depends on the amount of memory your **system** has and the number of graphics you incorporate: in a 640K-byte **system** , one file can be up to 150K bytes, which might be only six pages with...

...in from other word processing programs such as MultiMate, Word Perfect, and WordStar. Characters are **formatted** in two ways: the character **format** for whole paragraphs is defined by tags; within each paragraph, individual phrases can be **formatted** in any font and selectively kerned. A tag includes both character and paragraph **format** specifications: typeface, type size, type style, paragraph alignment, indentation, line spacing (leading), and tabs. The...

...the inclusion of a ruled line above, below, or around a paragraph.
Each different paragraph **format** used in a document must have a tag defined for it. Text brought in from a word processing program is automatically set in the font and **format** defined for the body-type tag: style specifications set up in compatible word processing programs...

...are overridden by the body-type tag specifications. You can change the font or the **format** for whole paragraphs by selecting paragraphs with ...

...Typedit, or convert ASCII text files created in other word processing programs. Otherwise, all text **formatting** and editing is done in the edit mode window; you cannot make changes to the text directly on the layout screen.

A **format** specification includes the typeface, type size, leading (spacing between lines), and paragraph alignment (such as left, centered, justified), plus degrees of kerning between letters. You can also set up a **format** specification to create a ruled line above a paragraph or to create an initial drop cap at the beginning of the paragraph. If you make changes to the **format** specifications after text is flowed onto a page, you need to reflow the text to convert it to the new specifications.

Each different character/paragraph **format** used in a document must have a **format** defined for it in the **format** file. This "style-sheet" feature makes Superpage well suited for producing a series of documents that use the same **format** , such as issues of a newspaper or magazine. You can open a new document and load the same **format** file you used in other documents. You can also change the type specifications by loading...

...coding, and final page composition are distributed among different departments or personnel.

A fully networked **system** with Superpage, Typedit, and Typeset includes a job tracking **system** that maintains a "job ticket" on each "file folder" and produces customized management reports.

A...to pay higher hourly rates for the levels of skill required to work with this **system** compared to the skill required to use the simpler packages.

Harvard Professional Publisher users will...

...they move up to Superpage, they will be able to convert their files to Superpage **format** and output them to a wide range of typesetters. This kind of upward compatibility will...

...low-end page composition products.

Photo: Superpage II menus aim for tight control of text **formatting** . Here, you are allowed to specify different leading **formats** for text lines between paragraphs and above subheads. Although the page-layout portion of Superpage II is WYSIWYG and more, the no-nonsense look of this **formatting** menu indicates that Superpage II addresses a different audience than the other products reviewed in...

21/3,K/13 (Item 13 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01204327 SUPPLIER NUMBER: 04630360 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Muscling in on the Mac: PC-based page composition. (desktop publishing, includes articles on IBM PC-to-Macintosh, fonts, PC equipment, and glossary of terms) (evaluation)
Burns, Diane; Venit, S.
PC Magazine, v6, p119(26)
Feb 10, 1987
DOCUMENT TYPE: evaluation LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 15423 LINE COUNT: 01171

... territory of the Apple Macintosh. Just over a year ago, when we first reviewed publishing **systems** on the PC (see "Words into Type: Meeting the Corporate Challenge' and "PCs and Typesetters...

...assumed that most desktop publishers would be unwilling to spend more on a page composition **system** than they spent on their database package and that they will be comparing their investment...handle long documents might seem clumsy in handling short documents with a lot of changing **formats** and that packages that handle short newsletters well might not be able to handle long...
...incorporating the following features:

The text for each article was imported from Microsoft Word (either

includes both character [redacted] paragraph **format** specificat[redacted]s: typeface, type size, type style, paragraph alignment, indentation, line spacing (leading), and tabs. The...

...the inclusion of a ruled line above, below, or around a paragraph.
Each different paragraph **format** used in a document must have a tag defined for it. Text brought in from a word processing program is automatically set in the font and **format** defined for the body-type tag: style specifications set up in compatible word processing programs...

...are overridden by the body-type tag specifications. You can change the font or the **format** for whole paragraphs by selecting paragraphs with the mouse and then clicking one of the...
...A more complex document will require more tags, one for each different combination of paragraph **format** , font, and tab settings. You can define function keys for commonly used tags to speed up the **formatting** process. The collection of tags defined for ...Ventura Publisher an excellent tool for producing a series of documents that use the same **format** (such as a series of newsletters or chapters in a book). The fact that the...

...s width and height must be stored in a width table for the document. Width **tables** are stored **in** **memory** while you are working on a document; the bigger the width table, the smaller the...

...style sheets may be Ventura's single most powerful feature, the fact that no paragraph **formats** may be assigned without a tag could be a drawback when dealing with some documents...

...can import scanned images if you have converted them to GEM or PC Paintbrush file **format** . Ventura Publisher can scale and crop bit-mapped images on the page. Menu selections let...Proprinter, Xerox's 4020 Color Ink Jet Printer or 4045 Laser Printer, and Tall Tree **Systems** ' JLaser printer card and compatible printers.
Ventura makes it easy to choose between different types...
...files, it offers a lot of the functionality previously available from only high-end WYSIWYG **systems** or code-based typesetting programs.
Ventura's ability to download fonts to the Laserjet and...

...displays the page in any of four views (full page, actual size, enlarged, or reduced). **Commands** are executed using **drop** -down menus, and all text editing and **formatting** is performed in an edit window. Harvard automatically updates the text files based on any...

...By making changes to the style sheet, you can effect global changes to the text **format** of your document.

21/3,K/14 (Item 1 from file: 47)
DIALOG(R)File 47:Gale Group Magazine DB(TM)

02949872 SUPPLIER NUMBER: 04975542 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Get the full EGA color spectrum. (enhanced graphics adapter)
Hummel, Robert L.
PC Magazine, v6, p311(14)
June 23, 1987
LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 6760 LINE COUNT: 00509

... in the EGA ROM BIOS and shown in Table E. The EGA BIOS provides for **changing** these values (as well as other **parameters**) by **accessing** them through a pointer. Our programs can **create** a new **table** **in** **memory** and, by aiming pointer at them, cause our parameters to become the default. The process...

...the way memory-resident programs attach themselves to interrupts the palette registers can also be **changed** individually through a BIOS call or by programming the Attribute Controller.

The EGA can produc[redacted].

21/3,K/15 (Item 2 from file: 47)
DIALOG(R)File 47:Gale Group Magazine DB(TM)

02945606 SUPPLIER NUMBER: 04995584 (USE FORMAT 7 OR 9 FOR FULL TEXT)
The ASYST software for scientific computing. (evaluation)
Hary, David; Oshio, Koichi; Flanagan, Steven D.
Science, v236, p1128(5)
May 29, 1987
CODEN: SCIEAS DOCUMENT TYPE: evaluation ISSN: 0036-8075
LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 5520 LINE COUNT: 00445

Scientists now use many software packagesthat have been adapted from mainframe and minicomputer **systems** to the personal computer (PC). Although such software packages were not developed specifically for the...

...1, 2, and 3 of ASYST (Table 2) and outlined the primary features of the **system** as well as some difficulties that we encountered in its use. Alternative software packages for...

...and Newman, Cambridge) have been discussed elsewhere whereas some other packages (for example, DADISP, DSP **Systems** , Cambridge) are relatively new and have not been extensively reviewed (2).

Programming Structure

Software for...

...are used, software development often involves laborious construction. Scientific programming is further complicated by programming **languages** that require a scalar algebra with numerous equations for the implementation of relations that are...

...to the plane of rotation of the ball) and velocity V vectors (3). In programming **languages** such as Fortran or BASIC, the vector product cannot be computed directly from the vector...

...file management utilities to store, retrieve, copy, delete, rename, print, and type DOS (disk operating **system**) files, all of which are supported by an on-line help facility.

Data manipulations in...

...to facilitate stack-oriented calculus, are available for the numeric and symbolic stacks. These include **commands** to duplicate or **drop** the top stack element, swap the top two elements, or display the contents of these ...

...scalar form. Complex scalars, vectors, or matrices in Cartesian (a ib) or polar (re(i)) **formats** are manipulated with specific words to compute the real (a) or imaginary (b) parts, magnitude...a negative real or integer number, or an integer or real number overflow) cause a " **system** restarted' message on the IBM PC-AT and an "illegal 8087 operation' message on the...

...thus far appears to belie the developers' claim that ASYST "provides a complete error trapping **system** with easy to understand error messages.'

Most of the 640-kbyte program and **systemmemory** of the IBM PC is required to run ASYST. The minimum size of the ASYST **system** is about 330 kbyte for modules 1 and 2. This includes the ASYST program, free...

...probably because integers (when not specifically terminated with a capital S) are in double-precision **format** (Fig. 1) and yield double-precision results when used as function operands. Thus the numeric ...

...times for seemingly nonapparent and uncontrollable reasons unless the informed programmer has carefully determined the **format** of the outcome of

each procedure used.
Column and multidimensional arrays arelimited to 64 Kbyte...on the IBM PC-AT. The documentation includes three manuals for the base and analysis **systems** and a manual for each additional module that is purchased. Maintenance of the ASYST software...with memory-resident programs that do not leave ASYST with enough space may hang the **system** and require a complete restart; user-defined function keys do not fully execute unless terminated...

...FILE1' DEFER> COPY TO FILE2 clears the symbol stack. Some problems depend on the particular **system** as well as the **system** software that is stored in read-only memory (BIOS ROM). For example, division by zero...

...these programs take control in response to a special key combination. For example, the DOS **GRAPHICS** .COM program stays **resident** and prints a **graphics** screen in response to the keys Shift-PrtSc. Because of the limited access to subdirectories...

...release of version 1.56 (10 December1986) excessive unusable memory was allocated to the ASYST **system** and increased the minimum **system** size from 330 to about 363 kbyte (modules 1 and 2) and 384 kbyte (modules 1, 2, and 3). This unusable memory space increases from 4% of the minimum **system** (version 1.53, modules 1 and 2) to 16% and is about 12% with all...

...of Southern California.
Table: 1. ASYST modules and prices.
Table: 2. ASYST versions, computers, operating **systems** , and peripherals tested. A math co-processor is required for the operation of ASYST. The...in BASIC, which uses line numbers as labels, is presented for comparison.
Photo: Fig. 4. **Schematic** representations of the acquisitionof multiple channels in the sequentially delayed timing mode. All n channels ...
CAPTIONS: ASYST modules and prices; versions, computers operating **systems** tested. (table); ASYST commands; word and equivalent BASIC subroutine. (table); Acquisition of multiple channels in...

21/3,K/16 (Item 1 from file: 636)

02550399 Supplier Number: 45144388 (USE FORMAT 7 FOR FULLTEXT)
BORLAND DELIVERS FIRST WINDOWS DATABASE ENGINE
M2 Presswire, pN/A
Nov 17, 1994
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 806

... of over 150 functions and advanced data integration services including: linked cursors; bidirectional scrollable cursors; **in - memory tables** ; Binary Large Object (BL0b) cache; debugging services; Structured Query **Language** (SQL) support; Query-by-Example (QBE) support; and support for **access** to **Open** Database Connectivity (ODBC) data sources. It is optimized for access from C, C++ and Pascal programs, although it can be accessed by any **language** capable of making calls to Microsoft Windows Dynamic Link Libraries (DLLs).
The Borland Database Engine...

21/3,K/17 (Item 2 from file: 636)

02527371 Supplier Number: 45092499 (USE FORMAT 7 FOR FULLTEXT)
PRODUCT BITS:BORLAND DEBUTS DATABASE ENGINE
Telecomworldwire, pN/A

Oct 28, 1994
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 160

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...new product is designed to provide robust database functionality and heterogeneous data connectivity to third- **generation language** application development. Borland says that its engine is the first standalone database engine that offers...

...over 150 functions and advanced data integration services including: linked cursors; bi-directional scrollable cursors; **in - memory tables** ; Binary Large Object (BLOb) cache; debugging services; Structured Query **Language** (SQL)support; Query-by-Example (QBE) support; and support for **access** to **Open** Database Connectivity (ODBC) data sources. It is optimized for access from C, C++ and Pascal programs, although it can be accessed by any **language** capable of making calls to Microsoft Windows Dynamic Link Libraries (DLLs).

21/3,K/18 (Item 3 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

02525293 Supplier Number: 45086539 (USE FORMAT 7 FOR FULLTEXT)
PRODUCT BITS:BORLAND DELIVERS WINDOWS DATABASE ENGINE
Telecomworldwire, pN/A
Oct 25, 1994
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 147

... The Engine is designed to provide robust database functionality and heterogeneous data connectivity to third- **generation language** application development, the Borland Database Engine 2.0 for Windows is the first standalone database...

...over 150 functions and advanced data integration services including: linked cursors; bi-directional scrollable cursors; **in - memory tables** ; Binary Large Object (Blob) cache; debugging services; Structured Query **Language** (SQL) support; Query-by-Example (QBE) support; and support for **access** to **Open** Database Connectivity (ODBC) data sources.

21/3,K/19 (Item 4 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

02512168 Supplier Number: 45052749 (USE FORMAT 7 FOR FULLTEXT)
BORLAND LAUNCHES DATABASE ENGINE 2.0 FOR WINDOWS DEVELOPMENT
Computergram International, n2518, pN/A
Oct 10, 1994
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 186

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...over 150 functions and advanced data integration services including linked cursors; bi -directional scrollable cursors; **in - memory tables** ; Binary Large Object cache; debugging services; Structured Query **Language** support; Query-by-Example support; and support for **access** to **Open** Database Connectivity data sources. Native SQL access extends the database range to include Oracle, Microsoft...

...s InterBase data. It [redacted] be accessed from C, C++ and P[redacted]al programs and any **language** capable of making calls to Microsoft Windows Dynamic Link Libraries

21/3,K/20 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

04411077 Supplier Number: 46471454 (USE FORMAT 7 FOR FULLTEXT)
Two Directions For SQL Server
InformationWeek, p89
June 17, 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Tabloid; General Trade
Word Count: 2988

... events
* Tight integration with Windows NT and BackOffice
* Can be controlled through OLE-capable development **languages** like Visual Basic
* New Distributed Transaction Coordinator based on X/Open TP monitor standard
* Bundled...

...of Sybase's notebookto-superserver database line.
Strengths:
* Portable; versions available for all major operating **systems** .
* One of four scalable DBMS products, including Sybase SQL Anywhere, Sybase IQ, Sybase MPP
* Gateways...

...Microsoft abandoned the OS/2 server platform in favor of its own Windows NT operating **system** , the two companies took the product in separate directions.
Two generations later, the progeny of...

...into the NT and BackOffice suite environments, Sybase continues to support a range of operating **systems** and hardware platforms. As a result, although SQL Server 6.5 and SQL Server 11...

...6.5 is World Wide Web integration.
The new Web Assistant tool helps users automatically **format** data from SQL Server databases into HTML pages. Web Assistant integrates SQL Server data into...

...to X/Open's XA standard for transaction monitors. So a transaction written under BEA **System** 's Tuxedo, IBM's Encina, or NCR's Top End can include SQL Server 6...

...Manager is its ability to manage remote servers as easily as a local SQL Server **system** . But it does not perform many of the DBA tasks involved in managing traditional "production...

...environments. For example, it doesn't effectively identify differences between databases in their data definition **languages** , or migrate DDL and stored procedures from test to production **systems** .
Administration Advances
Release 6.5 includes several other significant advances in ease of administration. The...

...great step forward that lets desktop programmers (rather than specialized DBAs) perform common database management **system** housekeeping tasks. The Assistant can't handle all DBA tasks, but it's a great...

...administration is SQL Distributed Management Objects, or SQL-DMO. It provides an interface between programming **languages** like Visual Basic and Visual C++, or any other **language** that supports OLE. You can use SQL-DMO

...to their applications[redacted] also requires administrative [redacted]pertise and understanding of the application's behavior. **System** 11 consolidates the configuration changes formerly accomplished by several means (sp configure, buildmaster, and dbcc...

...have to change parameters in a single configuration file, a major improvement over previous methods. **System** 11's SQL Server Manager tool provides the GUI to alter configuration parameters, while the...

...the NT package. SQL Server Manager (SSM) is the tool for managing local and remote **System** 11s. Its GUI panels support all major administrative tasks, such as security administration, object definitions...

...makes sense within the context of a company's requirements. SQL Server 6.5 and **System** 11 both exhibit strengths that will sway particular purchasers. The irony is that in spite...

...may differ from your own. According to SQL Server 6.5's documentation, Microsoft will **drop** support for some **command syntaxes** in the future. Also, while Microsoft has excellent homogeneous-transaction performance benchmarks, SQL Server 6...

...to prove its mettle under mixed workload torture tests.
Sybase's focused work on the **System** 11 engine promises strong performance for ad hoc workloads and environments that torture-test the...
...NetWare. Sybase's Replication Server replicates data from heterogeneous products like Oracle and DB2 into **System** 11 databases. Of course, it doesn't ship in the box with SQL Server 11...

21/3,K/21 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

03055083 Supplier Number: 44156971 (USE FORMAT 7 FOR FULLTEXT)
PLAYING TO WIN
HFD-The Weekly Home Furnishings Newspaper, v0, n0, p18
Oct 11, 1993
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1493

... Allen. If, down the road, those opportunities for growth are exhausted, he said, 'We may **change** our **charter** to say **residential** furnishings, which would **open** the door to **accessories** such as mirrors and lamps.'
The strategic vision behind LADD is clear: the $16 billion...

21/3,K/22 (Item 3 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

02938202 Supplier Number: 43972940
Merry Land & Investment Co., Inc. - Company Report
Investext, p1-14
July 16, 1993
Language: English Record Type: Abstract
Document Type: Magazine/Journal; Trade

ABSTRACT:
...in the 1980's and the problem-plagued savings and loan industry among others, have **created** an abundant supply of properties while buyers are relatively scarce due to the **limited** capital **available** for financing. Merry Land is in an excellent position to capitalize on the opportunities to...

...Land has raised $213 million of equity, of which $161 million has been

invested in **residential** apartments.
Tables in report: Stock Price, Earnings Data & Rating 1992-94; Assets 6/30/93; Apartment Properties...

21/3,K/23 (Item 1 from file: 624)
DIALOG(R)File 624:McGraw-Hill Publications

0364734
WRITING TO THE NET, KILLING PROCESSES BY NAME
Unix World November, 1991; Pg 137; Vol. VIII, No. 11
Journal Code: UNIX ISSN: 0739-5922
Section Heading: Wizard's Grabbag
Word Count: 2,107 *Full text available in Formats 5, 7 and 9*

BYLINE:
Dr. Rebecca Thomas

TEXT:
... called "Yellow Pages"). This script also runs on our older Silicon Graphics Iris machines under **System** V, which don't use NIS.

Doctor's explanation of writenet operation. First, line 5...

... maintaining an extra file, it avoids changing the source code for the script itself. A **system** administrator or operator may know how to edit a file, but may not know shell programming **syntax** .

The exclusion list file path name is stored in the EXCLUDELIST variable so it only...

... recognizes different option sets. To determine the UNIX version, test the name of the operating **system** kernel: if it's /vmunix, a BSD or SunOS ps command is being used, otherwise...

... of running ps to list all processes, selecting the appropriate candidates, then constructing the proper **kill command** line. If you run zap carelessly you could terminate processes by mistake, but if you... convenient processing. Usage defines the correct usage message to invoke the script. The "preamble" section **ends** with the trap **command** which arranges for erasure of the temporary file when the script terminates.

Next, command-line...

... processed with the getopts() routine, if it's available. This library routine supports the Command **Syntax** Standard, which I encourage so UNIX utilities have a consistent command-line **syntax** . The getopts() function is explained in my August 1991 column, so I won't repeat...

...the Pattern variable (line 51).

The "if" test in lines 56-60 determines whether the **system** is BSD-derived. Lines 62-66 determine the "flavor" of the echo command-one flavor...

...2, and so on. The second field is referenced by line 85, which is the **kill command** line used to actually signal the designated process. After all selected ps entries have been...

... it is already dead and exists as a zombie process, which still has a kernel- **resident** process **table** entry although all other resources have been deallocated. This occurs when the process' parent process...

...Submissions

Mail Bourne/Korn shell scripts, C programs, or tips to ease the burden of **system** administrators, programmers, and users to "Wizard's Grabbag,"

UNIXWORLD, 444 Castro St...

SPECIAL FEATURE:
...rwall -h $Hostlist
B. Contents of a sample /etc/hosts file:
Host Database for Opus **Systems** ' SPARC Clone (yin)
SunOS 4.1.1 Version 5
If the NIS is running,
this... of zap to terminate a hung editor process running on a virtual terminal. (On this **system** the virtual terminal devices are named /dev/vt01 through /dev/vt08). The regular expression pattern...

21/3,K/24 (Item 2 from file: 624)
DIALOG(R)File 624:McGraw-Hill Publications

0106821
Pixels on the March : The 8514/A and Artist 10 MC graphics coprocessor boards for the IBM PS/2s
; Pg 201; Vol. 14, No. 1
Section Heading: Reviews
Word Count: 3,250 *Full text available in Formats 5, 7 and 9*

BYLINE:
Bradley Dyck Kliewer

TEXT:
Fast, high-resolution graphics **systems** were once the domain of computer-aided drafting and design (CADD) and specialized image-processing ...

...science and engineering. However, the past few years have shown advances in desktop publishing, multitasking **systems** , and business graphics, and these advances are pushing the limits of personal computer graphics standards...

...at two graphics coprocessors for the IBM PS/2 Micro Channel architecture (MCA) computers. The **system** I used was a 16-MHz IBM PS/2 Model 80-071 running IBM DOS...

... only one at a time; this severely restricts its potential for use in desktop publishing **systems** .

The 8514/A adapter includes 512K bytes of graphics memory (unlike memory on the CGA...

...a copy under a special agreement and will use direct hardware control in its operating- **system** products. To date, only Microsoft Windows/286 uses the direct hardware interface; an 8514/A...surrounding borders, you must send a begin-area command, outline the area, and send an **end** -area **command** . This in itself would not be much of a problem, but each polygon or polyline...

... circle drawing benchmark. Editor's note: The benchmark programs are available in a variety of **formats** . See page 3 for details. To fill the circle, all points have to be calculated...

... incorporate any examples of program code, although it comes with a demonstration program and C **language** interface code (including source code for the demonstration program) on a disk. Information about the...

...program is running. Thus, software written for the EGA and VGA will work on the **system** . If you connect a second monitor to the VGA output, the VGA display continues normal...

...can use graphics modes simultaneously.

Artist 10 MC

In contrast to the 8514/A, Control **Systems** ' Artist 10 MC is a much more powerful (and, at $3695 and $3995, much more...

...the reviewed configuration). The colors are selectable from a palette of 16.7 million. Control **Systems** does not make a 16- to 256-color upgrade kit.

At this time, the only...

... packages the Artist 10 MC supports are AutoCAD release 9 and VersaCAD. According to Control **Systems** , drivers for Microsoft Windows are under development, but they were not yet available at the...make a more permanent record of the initialization file.

Programming the Artist 10 MC

Control **Systems** ' Technical Reference manual covers its family of Artist 10 Series of graphics controllers. The manual...

... programming reference. The only source code in the manual covers DMA transfers with the host **system** .

The manual's information is sometimes out of date with regard to the Artist 10...

...I was able to find the correct address with the aid of a debugger.

Control **Systems** also supplies a handy program called HITDUMP, which dumps the contents of the ACRTC registers...

... VGA through to the high-resolution monitor. When the Artist 10 MC is in its **resident - graphics** modes, the PS/2's VGA output continues to display. Once again, I was able...drivers are for the best-selling PC CADD programs (and its price brings the entire **system** into the graphics workstation range). It is also a very well documented adapter, although it ...

...Installation Guide
Price
$1350
Artist 10 MC Type
IBM PS/2 graphics adapter
Company
Control **Systems**
2675 Patton Rd.
P.O. Box 64750
St. Paul, MN 55164
(612) 631-7800
Features...

21/3,K/25 (Item 1 from file: 484)
DIALOG(R)File 484:Periodical Abs Plustext

04099566 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Portable embedded C
Holtzman, Jeff
Electronics Now (GRAD), v70 n2, p6-8+, p.4
Feb 1999
ISSN: 1067-9294 JOURNAL CODE: GRAD
DOCUMENT TYPE: Feature
LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 2094

...ABSTRACT: standards, can be altered to reduce the negative effects that

result whenever the C pr[redacted]amming **language** meets embedd[redacted] **systems** . The portable embedded C model is discussed.
TEXT:
IT SEEMS THAT WHENEVER THE C PROGRAMMING **LANGUAGE** BUMPS UP AGAINST THE WORLD OF EMBEDDED **SYSTEMS** , SOMETHING GROTESQUE USUALLY EMERGES. ALL SORTS OF NONSTANDARD **LANGUAGE** EXTENSIONS APPEAR, WHICH HAS several effects.
First, any hope of portability is shot This means...

...incompatibilities.
What if you could reduce those effects? What if you could have a standard **language** that covered most of what people do in embedded **systems** ? What if you could increase your code reuse factor from maybe 20% to 80% or even more? And what if you could do it all in a widely used **language** ?
Suppose you took Standard C, as defined by ANSI and ISO standards, and added to and subtracted from it to achieve an embedded- **systems** control **language** . Well, you might ask, hasn't that been already done lots of times? Doesn't...

...alter the paradigm a little. Most C implementations adapted for embedded use take the core **language** , then add all sorts of proprietary extensions to handle specific capabilities of the specific target...

...Suppose we abstract certain common features out in a platform-independent way. Then we use **language** itself to mask the differences. But how can you do that with such a wide...

...that remains true to the spirit of C, but is optimized for use with embedded **systems** , yet is not tied to any one microcontroller device or architecture. The following is a start on my design for such a **language** .
Modeling Memory
Standard C has a very weak model of the actual hardware that it...

...of RAM or four physically separate address spaces. C doesn't care. Typical non-embedded **systems** use that type of layout in RAM, where the size of the static and code...

...careful design and testing are required to ensure that they never overlap.
But in embedded **systems** programming, we do care about those kinds of things, and more. For example, most embedded **systems** put a premium on RAM. Program code must execute from some sort of read-only...

...point here is to acknowledge explicitly the existence of these types of memory and provide **language** -level support for them. Doing so has a subtle but liberating effect. It allows you...

...could define average as an integer that is stored in RAM: (Formula Omitted)
From a **language** standpoint, this cleans up the messy process of reading from and writing to EEPROM. Let...

...table of addresses, one each for each interrupt supported by the device.
From a C **language** point of view, an interrupt vector table ... functions. The catch is that we need to be able to specify the exact location **in** **memory** where the **table** is located (as well as the type of memory). Often the table begins at location...

...Standard C provides a simple means of initializing an array, as follows: (Formula Omitted)
That **syntax** tells the compiler to put the addresses of f1, f2, and into the first three...

...an array of integers, as declared. It's really an array of function pointers. The **syntax** is messy and is left as an exercise for interested readers.
Now we can declare...

...However, a specific platform may limit it to only one or two. Our embedded C **language** must therefore provide a means of specifying where executable code is to be located. With...

...which is intended to handle platform specifics. Using #pragma increases portability, but clutters up the **syntax** . A related issue is whether to create three directives (one for each type of memory), or one directive with parameters. I really dislike cluttered **syntax** , but I have made a commitment to minimizing changes to the **language** . So let's use #pragma and parameters. The complete **syntax** is: (Formula Omitted)
where code refers to executable code, data refers to constant data, and...

...monitor might do nothing, cycle on and off for a while, power up and then **shut down** in an **endless** cycle-or at least for a while. Then it comes on and operates normally until...That's it for now. Next month we'll explore the exciting world of deflection **system** failures! Until then, check out my Web site, www.repairfaq.org. I welcome comments (via...

DESCRIPTORS: C **language** ;

21/3,K/26 (Item 1 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00889937 95-39329
Basics of motion control
Anonymous
Machine Design v66n12 PP: 6-26 Jun 1994
ISSN: 0024-9114 JRNL CODE: MDS
WORD COUNT: 4575

...ABSTRACT: from one point to another, or precisely constraining the speed, acceleration, and positioning of a **system** throughout a move. An overview of motion control techniques is presented that puts each technique ...
...TEXT: and control of both velocity and position, they need a controller to keep track of **system** operating conditions at any given time. This controller can be either hardwired electronic logic, a computer, or a PLC.

In general, the simplest positioning **system** of this sort might be found on older milling machines. These contain an x-y positioning **system** for moving the fixture holding the workpiece. The positioning **system** involves ac or dc motors, an adjustable-speed drive, clutch, and a position transducer that reads out the position of each table axis. The positioning mechanism for such a **system** is usually a ball screw.

Many **systems** for point-to-point positioning use a stepping motor which is considered particularly well suited...

... through software. The computer controls the time period between control pulses using precalculated constants stored **in memory tables** . These constants may be optimized empirically by running various motor velocity versus time trials.

No...

... deceleration profile and motor velocity (stopping frequency) through empirically testing various profiles.

Once acceleration/deceleration **tables** have been stored **in memory** , a software routine uses the table values to generate motor-control pulses at proper frequencies...

...be contrasted with point-to-point control by first examining some of the shortcomings of **systems** powered by the latter approach. In the simplest

... algorithm coefficien[redacted]in real time to compensate for[redacted]riations in the environment or in the **system** itself. In general, the controller periodically monitors the **system** transfer function and then modifies the control algorithm. It does so by simultaneously learning about...

...is to make the controller robust to a point where the performance of the complete **system** is as insensitive as possible to modeling errors and to changes in the environment.

Even ordinary feedback-control **systems** are adaptive in a limited sense, in that they can compensate for changes at their input that are within the **system** bandwidth. But these changes are comparatively small. Such **systems** can become unstable for large input swings, or may simply be unable to compensate for...

... reference adaptive control (MRAC) and self-tuning regulators (STRs). In MRAC, a reference model describes **system** performance. The adaptive controller is then designed to force the **system** or plant to behave like the reference model. Model output is compared to the actual...

21/3,K/27 (Item 2 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00751951 94-01343
Gas consumption in the United States 1991
Anonymous
Gas Energy Review v21n7 PP: 15-20 Jul 1993
ISSN: 8756-5471 JRNL CODE: GER
WORD COUNT: 1938

...TEXT: from 31.5% in 1990. These continuing large increases can be attributed to the additional **availability** of **open access** transportation (and also in part to improved reporting). These volumes were utilized by all customer classes: 68.8% by industrial, 23.8% by electric utilities for power **generation** and the balance by commercial and **residential** customers. **Table** 3(**Table** 3 omitted) shows a breakdown of the transport gas by class of service.

COGENERATION

Natural...

21/3,K/28 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01094881 CMP ACCESSION NUMBER: IWK19960617S0072
Product Review - Two Directions For SQL Server - Microsoft's and Sybase's versions of the database management system **for Windows NT have a common origin but different personalities**
Howard Fosdick
INFORMATIONWEEK, 1996, n 584, PG89
PUBLICATION DATE: 960617
JOURNAL CODE: IWK LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: InformationWeek Labs
WORD COUNT: 2634

...**Two Directions For SQL Server - Microsoft's and Sybase's versions of the database management** system **for Windows NT have a common origin but different personalities**
TEXT:
... Microsoft abandoned the OS/2 server platform in favor of its own Windows NT operating **system** , the two companies took the product in separate directions. - Two generations later, the progeny of...

...into the NT and BackOffice suite environments, Sybase continues to support a range of operating **systems** and hardware platforms. As a result, although SQL Server 6.5 and SQL Server 11...
... 6.5 is World Wide Web integration.

The new Web Assistant tool helps users automatically **format** data from SQL Server databases into HTML pages. Web Assistant integrates SQL Server data into...

...to X/Open's XA standard for transaction monitors. So a transaction written under BEA **System** 's Tuxedo, IBM's Encina, or NCR's Top End can include SQL Server 6...

...Manager is its ability to manage remote servers as easily as a local SQL Server **system** . But it does not perform many of the DBA tasks involved in managing traditional " production...

...environments. For example, it doesn't effectively identify differences between databases in their data definition **languages** , or migrate DDL and stored procedures from test to production **systems** .

Administration Advances

Release 6.5 includes several other significant advances in ease of administration. The...

...great step forward that lets desktop programmers (rather than specialized DBAs) perform common database management **system** housekeeping tasks. The Assistant can't handle all DBA tasks, but it's a great...

...administration is SQL Distributed Management Objects , or SQL-DMO. It provides an interface between programming **languages** like Visual Basic and Visual C++, or any other **language** that supports OLE. You can use SQL-DMO in programs written in these **languages** to manipulate SQL Server through OLE automation. This is a major improvement, since SQL Server (and NT) previously lacked a scripting **language** . SQL Server 6.5 also now supports the Simple Network Management Protocol, so network management
...friendliness and integrating its DBMS with other products, Sybase focused on entirely different areas in **System** 11: performance and quality.

The old SQL Server 4.x product (from which both SQL Server 6.5 and **System** 11 are descended) was an excellent DBMS for early client- server applications and transaction servers...

...that time-DB DROP, as in dropping the entire database. Sybase made numerous improvements in **System** 10. But the consensus was that these enhancements did not address the two preeminent user concerns-performance and quality.

With **System** 11, Sybase focused on correcting these shortcomings. The company **systematically** analyzed the DBMS for performance, scalability, and mixed workload constraints, and then changed internals as...

...within the guidelines of the ISO-9001 quality standards.

Sybase made a major change in **System** 11's memory management. Avoiding real disk I/O is the key to speed in...

...are assigned to specific tables. This not only increases performance, but also lets DBAs tailor **System** 11's I/O performance priorities. Critical "reference" **tables** can be held **in** **memory** , for example. Along with cache size and object relationship, you can set different block sizes for different caches, ranging from 2 Kbytes up to 16 Kbytes, or you can let **System** 11 dynamically determine block size for you. Larger block I/O sizes significantly speed table scans because disks incur little overhead for reading larger blocks. **System** 11 combines large I/Os with "sequential prefetch" of pages for higher performance in queries...

...out" less frequently by long-running queries. This protects OLTP response time from decision support **system** queries. DBAs can configure

this behavior. A new "housekeeper" task cleverly uses idle CPU cycles... ...wash" the buffers and keep them optimized.

Sybase rewrote much of the query optimizer for **System** 11. Unlike some DBMS upgrades, there are few reports of "negative progress," where a query that ran well under **System** 10 runs poorly under **System** 11. This is critical to existing users who want to upgrade to **System** 11, because it vastly reduces effort to upgrade when you can trust that negative progress queries won't pop up. **System** 11 also offers an easier upgrade for existing users than did **System** 10. The online upgrade documentation is improved, too.

Reduced Contention

System 11 enhances internal DBMS locking via the Parallel Lock Manager (PLM). As **System** 11 removes contention for buffer space by named caches, so it reduces symmetric multipro-cessing...

...problem is "insert contention"- INSERTs that compete for pages at the end of a table. **System** 11 can slice non-clustered tables into data partitions. This reduces last- page contention for parallel INSERTs and increases performance.

System 11 has several restrictions on data partitioning: It does not work for transaction logs; indexes...

...placeobject). Like Microsoft's Dynamic Locking Architecture, **System** 11 partitioning is effective when it applies. But it only applies to certain situations.

A complaint about **System** 10 was that the work on SMP machines was not balanced among CPUs. Instead, **System** 11's kernel is symmetric, and distributes network I/O equally. The PLM plays a role in this. Sybase calls its SMP design Virtual Server Architecture (VSA). With **System** 11's transparent Multiple Network Engine feature, VSA finally achieves its full potential.

As these internal changes imply, Sybase vastly enhances the DBMS' configurability in **System** 11. **System** 11 has more than 120 configuration variables, while SQL Server 6.5 remains at less...

...to their applications. It also requires administrative expertise and understanding of the application's behavior. **System** 11 consolidates the configuration changes formerly accomplished by several means (sp ...have to change parameters in a single configuration file, a major improvement over previous methods. **System** 11's SQL Server Manager tool provides the GUI to alter configuration parameters, while the...

...the NT package. SQL Server Manager (SSM) is the tool for managing local and remote **System** 11s. Its GUI panels support all major administrative tasks, such as security administration, object definitions ...

...makes sense within the context of a company's requirements. SQL Server 6.5 and **System** 11 both exhibit strengths that will sway particular purchasers. The irony is that in spite...

...may differ from your own. According to SQL Server 6.5's documentation, Microsoft will **drop** support for some **command syntaxes** in the future. Also, while Microsoft has excellent homogeneous- transaction performance benchmarks, SQL Server 6...

...to prove its mettle under mixed workload torture tests.

Sybase's focused work on the **System** 11 engine promises strong performance for ad hoc workloads and environments that torture-test the...

...NetWare. Sybase's Replication Server replicates data from heterogeneous products like Oracle and DB2 into **System** 11 databases. Of course, it doesn't ship in the box with SQL Server 11...

21/3,K/29 (Item 1 from file: 148)

08918837 SUPPLIER NUMBER: 18535883 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Adaptive reset control offers faster temperature recovery. (extruder barrel temperature control)
Kramer, William A.
British Plastics & Rubber, p4(3)
May, 1996
ISSN: 0307-6164 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 1950 LINE COUNT: 00154

TEXT:

...delays in response during steady operation, calling for some sort of compensation by the control **system** . But when the extruder stops and starts the control **system** can be fooled in making completely the wrong adjustments. William A Kramer of Davis-Standard...

...a controller incorporating self-learning logic which returns to normal running more quickly than established **systems** .
... the extrusion industry due to its importance to the process. Extruders have heating and cooling **systems** on their barrels for two basic reasons: first, to provide for heat-up and to...
...fact do not control the inner surface, or supply proper deep thermocouples with sluggish control **systems** (2).

An alternative **system** that uses two thermocouples was developed and patented several years ago(3). This monitors the...

...of 'instantaneous derivative'. Reset is still achieved through a conventional automatic function. The dual thermocouple **system** has proven to be superior to PID **systems** in stability(4), but with little or no advantage in upset recovery time.

One of...

...of string-up, change over or splicing, or during an unplanned event such as a **shut down** or emergency **stop** . Barrel temperature upsets occur due to the change in process load that results at the...

...results of a development programme initiated with the purpose of creating a barrel temperature control **system** that could quickly return to a previous stable condition by somehow 'remembering' where it was...

...and patented by Davis-Standard(5). Based on the proven dual thermocouple principle, the new **system** has added an internal look-up **table in memory** of reset values versus screw speeds. This table is learned automatically as the extruder is...

...applied whenever screw speed changes. This action works as a sort of 'instantaneous integral'. The **system** provides fast response, accuracy and stability and for the first time, a positive method for...

...cooling as well as high heating during the development and testing of the new control **system** .

This article presents the results of a series of trials on the 114 mm, 24...

...L:D water-cooled extruder with a DSB barrier screw and an EPIC II control **system** with data acquisition capabilities. All trials were run using a 0.9 MI film grade...

...The latter two control schemes were both run in Davis-Standard's EPIC II control **system** . During the dual thermocouple trial Adaptive Reset action was disabled, but the **system** 'learned' the reset values for the screw speeds that were applied during the final trial...2. These are the values that were learned and applied by the Adaptive Reset control **system** during the trials. The feed area, zone 1, shows a heating requirement at low speed ...
...control thermocouple values over time during the three repeated trials with the three different control **systems** on the time scale from the first run. Figures 3 and 4 are of zone...

...appears to be much slower in reaction and never reaches set point. The other two **systems** behave in a similar way to zone 1, with the superior performance of Adaptive Reset...

...quick recovery to set point can have on the process. In both cases, the new **system** brought the melt temperature back to a stable condition in about half the time.
Conclusions...

...being very slow to get to set point.
The newly-developed Adaptive Reset temperature control **system** is shown to give dramatic improvement in response to screw speed changes and start-stop...

...to screw speed. It also exhibits the excellent stability inherent in the dual thermocouple control **system** .
References
1 - R F Bayless, SPE Antec Technical Papers, pg 544, 1978.
2 - H E...

21/3,K/30 (Item 2 from file: 148)

08911910 SUPPLIER NUMBER: 18592180
Extruder temperature control with adaptive reset. (heating control for extrusion barrels linked to screw speed) (includes bibliography)
Kramer, William A.
Rubber World, v214, n4, p19(4)
July, 1996
ISSN: 0035-9572 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 1850 LINE COUNT: 00148

...ABSTRACT: new process for effectively controlling the temperature of extruder barrels links a barrel's heating **system** to the speed of its screw. The process is based on the observation that the...

...an extruder barrel becomes. By adjusting quickly and accurately to temperature control needs, the new **system** , called adaptive reset, is a considerable improvement over previous **systems** , which reacted to conditions after they changed.

TEXT:
...the extrusion industry due to its importance to the process. Extruders have heating and cooling **systems** on their barrels for two basic reasons. First, to provide for heat-up and to...
... fact do not control the inner surface, or supply proper deep thermocouples with sluggish control **systems** (ref. 2).
An alternate **system** that utilizes two thermocouples was developed and patented several years ago (ref. 3) that monitors...

...of instantaneous derivative. Reset is still achieved through a conventional automatic function. The dual thermocouple **system** has proven to be superior to PID **systems** in stability (ref. 4), but with little or no advantage in upset recovery time.
Objective...

...of string-up, change-over or splicing, or during an unplanned event such as a **shut - down** or emergency **stop** . Barrel temperature upsets occur due to the change in process load that results at the...

...results of a development program initiated with the purpose of creating a barrel temperature control **system** that could quickly return to a previous stable condition by somehow remembering where it was...

...developed, tested and patented (ref. 5). Based on the proven dual

thermocouple principle, [redacted] new **system** has added an int[redacted]al look-up **table in memory** of reset values versus screw speeds. This table is automatically learned as the extruder is...

...applied whenever screw speed changes. This action works as a sort of instantaneous integral. The **system** provides fast response, accuracy and stability, and for die first time, a positive method for...

...cooling as well as high heating during the development and testing of the new control **system** .
This article presents the results of a series of trials on the 114 mm, 24...

...L/D water-cooled extruder with a DSB barrier screw and an EPIC II control **system** with data acquisition capabilities. All trials were run using a 0.9 melt index (MI...

...auto-tuned. The latter two control schemes were both run in the EPIC II control **system** . During the dual thermocouple trial, adaptive reset action was disabled, but the **system** learned the reset values for the screw speeds that were applied during the final trial...2. These are the values that were learned and applied by the adaptive reset control **system** during die trials. The feed area, zone 1, shows a heating requirement at low speed ...
...control thermocouple values over time during the three repeated trials with the three different control **systems** on the time scale from the first run. Figures 3 and 4 are of zone...

...load, appears to be much slower in reaction and never reaches setpoint. The other two **systems** behave similar to zone 1, with the superior performance of adaptive reset obvious. The affect...

...a quick recovery to setpoint can have on the process. In both cases, the new **system** brought the melt temperature back to a stable condition in about half the time.
Conclusions...

...5, being very slow to get to setpoint.
The newly developed adaptive reset temperature control **system** is shown to give dramatic improvement in response to screw speed changes and start-stop...

...to screw speed. It also exhibits the excellent stability inherent to die dual thermocouple control **system** . It offers extrusion processors significant improvements in quality and efficiency at no significant increase in...

21/3,K/31 (Item 3 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

08758136 SUPPLIER NUMBER: 18409885 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Two directions for SQL Server. (Microsoft's SQL Server 6.5 DBMS and Sybase's SQL Server 11 for Windows NT DBMS) (Software Review) (Evaluation)
Fosdick, Howard
InformationWeek, n584, p89(5)
June 17, 1996
DOCUMENT TYPE: Evaluation ISSN: 8750-6874 LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 3136 LINE COUNT: 00260

...ABSTRACT: s SQL Server for Windows NT 11.0 DBMS is designed for performance and quality. **System** 11's Logical Memory Manager allows users to reduce real disk I/O. The product...

...configuration variables. It also includes the SQL Server Manager tool and a SQL Monitor client. **System** 11 costs $3,595 for an eight-user

license and $34,995 for [redacted] unlimited...
... events
* Tight integration with Windows NT and BackOffice
* Can be controlled through OLE-capable development **languages** like Visual Basic
* New Distributed Transaction Coordinator based on X/Open TP monitor standard
* Bundled...

...of Sybase's notebookto-superserver database line.
Strengths:
* Portable; versions available for all major operating **systems** .
* One of four scalable DBMS products, including Sybase SQL Anywhere, Sybase IQ, Sybase MPP
* Gateways...

...Microsoft abandoned the OS/2 server platform in favor of its own Windows NT operating **system** , the two companies took the product in separate directions.
Two generations later, the progeny of...

...into the NT and BackOffice suite environments, Sybase continues to support a range of operating **systems** and hardware platforms. As a result, although SQL Server 6.5 and SQL Server 11...

...6.5 is World Wide Web integration.
The new Web Assistant tool helps users automatically **format** data from SQL Server databases into HTML pages. Web Assistant integrates SQL Server data into...

...to X/Open's XA standard for transaction monitors. So a transaction written under BEA **System** 's Tuxedo, IBM's Encina, or NCR's Top End can include SQL Server 6...

...Manager is its ability to manage remote servers as easily as a local SQL Server **system** . But it does not perform many of the DBA tasks involved in managing traditional "production...

...environments. For example, it doesn't effectively identify differences between databases in their data definition **languages** , or migrate DDL and stored procedures from test to production **systems** .
Administration Advances
Release 6.5 includes several other significant advances in ease of administration. The...
...great step forward that lets desktop programmers (rather than specialized DBAs) perform common database management **system** housekeeping tasks. The Assistant can't handle all DBA tasks, but it's a great...

...administration is SQL Distributed Management Objects, or SQL-DMO. It provides an interface between programming **languages** like Visual Basic and Visual C++, or any other **language** that supports OLE. You can use SQL-DMO in programs written in these **languages** to manipulate SQL Server through OLE automation. This is a major improvement, since SQL Server (and NT) previously lacked a scripting **language** . SQL Server 6.5 also now supports the Simple Network ...friendliness and integrating its DBMS with other products, Sybase focused on entirely different areas in **System** 11: performance and quality.
The old SQL Server 4.x product (from which both SQL Server 6.5 and **System** 11 are descended) was an excellent DBMS for early client-server applications and transaction servers...

...that time-DB DROP, as in dropping the entire database. Sybase made numerous improvements in **System** 10. But the consensus was that these enhancements did not address the two preeminent user concerns--performance and quality.
With **System** 11, Sybase focused on correcting these shortcomings. The company **systematically** analyzed the DBMS for performance, scalability, and mixed workload constraints, and then changed internals as...

```
Set     Items   Descript
S1         19   TEFP? OR TEFPFEC OR EXTEND?()FAST()PATH?
S2     332852   PERSISTENT? OR RESIDENT? OR "IN"()(MEMOR? OR SRAM OR RAM) -
             OR TSR
S3       1143   S2(3N)(TABLE? OR GRAPH? OR CHART? OR TUPL? OR MATRIX? OR M-
             ATRICE?)
S4   14995962   SYNTAX? OR FORMAT? OR LANGUAGE? OR SCHEMA? OR SYSTEM?
S5      65427   (ACCESS? OR AVAILAB?)(4N)(LIMIT? OR PARAMET? OR OPEN OR CL-
             OSED OR PARTIAL? OR TIER? OR HIERARCH?)
S6        485   S3 AND S4
S7        885   (DROP? OR END? OR KILL? OR STOP?)(3N)(COMMAND? OR SHUTDOWN?
              OR POWERDOWN OR (POWER OR SHUT)()(DOWN OR OFF))
S8          2   S6 AND S5
S9          2   S5 AND S6
S10       115   S3(10N)S4
S11        46   S10 AND (GENERAT? OR CREAT? OR MODIF? OR CHANGE? OR ALTER?
              OR REGENERAT? OR RECREAT? OR AUTHOR)
S12         0   S7 AND S3
S13         8   S1 AND (S4 OR S5 OR S7)
S14         0   S1 AND S3
S15        56   S8 OR S9 OR S11 OR S13
S16        49   S15 NOT PY>1999
S17        48   S16 NOT PD>19990812
File   8:Ei Compendex(R) 1970-2002/Sep W3
         (c) 2002 Engineering Info. Inc.
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         (c) 2002 Cambridge Sci Abs
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         (c) 2002 Cambridge Scient. Abstr
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         (c) 2002 ProQuest Info&Learning
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         (c) 2002 Info.
File   6:NTIS 1964-2002
         (c) 2002 NTIS,                                       Res
File 144:Pascal 1973-20
         (c) 2002 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2002/Sep W5
         (c) 2002 Inst for Sci Info
File  95:TEME-Technology & Management 1989-2002/Sep W4
         (c) 2002 FIZ TECHNIK
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Bibliographic Databases

17/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05494515 E.I. No: EIP00025060259
Title: Study on the development of transmission-type extrinsic Fabry-Perot interferometric optical fiber sensor
Author: Kim, Sang-Hoon; Lee, Jung-Ju; Lee, Dong-Chun; Kwon, Il-Bum
Corporate Source: Korea Advanced Inst of Science and Technology, Taejon, S Korea
Source: Journal of Lightwave Technology v 17 n 10 1999. p 1869-1874
Publication Year: 1999
CODEN: JLTEDG ISSN: 0733-8724
Language: English
Document Type: JA; (Journal Article) Treatment: G; (General Review)
Journal Announcement: 0004W4
Abstract: The conventional reflection-type extrinsic Fabry-Perot interferometric (EFPI) optical fiber sensor has good sensitivity and resolution compared with other types of optical fiber sensors. However, they have the disadvantage that the distinction of strain direction of EFPI is difficult because of measurement method by only fringe counting. This paper presents the newly developed transmission-type EFPI (**TEFPI**) optical fiber sensor, which has been improved by additional functions, and whose measuring **system** differs from that of the reflection-type EFPI optical fiber sensors using a single-mode fiber (SMF) and multimode (MMF) fibers as light guides and reflectors, respectively. The output signal of the **TEFPI** optical fiber sensor was analyzed with the uniform plane wave-based model, the SMF power distribution-based model and the splice loss-based model; the analyzed signals were then verified experimentally. Based on the results of analysis, the **TEFPI** optical fiber sensor was fabricated using two single-mode fibers connected to the light source and optical receiver; this was then used in strain measurement. The strain measured by the **TEFPI** optical fiber sensor was compared with that measured by the electric strain gauge. (Author abstract) 16 Refs.
Descriptors: *Fiber optic sensors; Fabry-Perot interferometers; Light transmission; Photosensitivity; Optical resolving power; Strain measurement ; Single mode fibers; Multimode fibers; Light sources; Strain gages
Identifiers: Uniform plane wave based model; Optical receiver; Transmission type extrinsic Fabry Perot interferometric; Electrical strain gauge
Classification Codes:
741.1.2 (Fiber Optics)
741.1 (Light/Optics); 941.3 (Optical Instruments); 943.2 (Mechanical Variables Measurements); 943.1 (Mechanical Instruments); 942.1 (Electric & Electronic Instruments)
741 (Optics & Optical Devices); 941 (Acoustical & Optical Measuring Instruments); 943 (Mechanical & Miscellaneous Measuring Instruments); 942 (Electrical & Electronic Measuring Instruments)
74 (OPTICAL TECHNOLOGY); 94 (INSTRUMENTS & MEASUREMENT)

17/5/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05371330 E.I. No: EIP99094775914
Title: Recursive array layouts and fast parallel matrix multiplication
Author: Chatterjee, Siddhartha; Lebeck, Alvin R.; Patnala, Praveen K.; Thottethodi, Mithuna
Corporate Source: Univ of North Carolina, Chapel Hill, NC, USA
Conference Title: Proceedings of the 1999 11th Annual ACM Symposium on Parallel Algorithms and Architectures, SPAA'99
Conference Location: Saint-Malo Conference Date: 19990627-19990630
Sponsor: ACM SIGACT; ACM SIGARCH
E.I. Conference No.: 55445
Source: Annual ACM Symposium on Parallel Algorithms and Architectures 1999. p 222-231
Publication Year: 1999

CODEN: AASAES
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 9911W1
Abstract: Matrix multiplication is an important kernel in linear algebra algorithms, and the performance of both serial and parallel implementations is highly dependent on the memory system behavior. Unfortunately, due to false sharing and cache conflicts, traditional column-major or row-major array layouts incur high variability **in memory system** performance as **matrix** size varies. This paper investigates the use of recursive array layouts for improving the performance of parallel recursive matrix multiplication algorithms. We extend previous work by Frens and Wise on recursive matrix multiplication to examine several recursive array layouts and three recursive algorithms: standard matrix multiplication, and the more complex algorithms of Strassen and Winograd. We show that while recursive array layouts significantly outperform traditional layouts (reducing execution times by a factor of 1.2-2.5) for the standard algorithm, they offer little improvement for Strassen's and Winograd's algorithms; we provide an algorithmic explanation of this phenomenon. We demonstrate that carrying the recursive layout down to the level of individual matrix elements is counter-productive, and that a combination of recursive layouts down to canonically ordered matrix tiles instead yields higher performance. We evaluate five recursive layouts with successively increasing complexity of address computation, and show that addressing overheads can be kept in control even for the most computationally demanding of these layouts. Finally, we provide a critique of the Cilk system that we used to parallelize our code. (**Author** abstract) 41 Refs.
Descriptors: *Parallel processing systems; Parallel algorithms; Matrix algebra
Identifiers: Parallel matrix multiplication; Strassen's algorithm; Winograd's algorithms; Recursive array layouts
Classification Codes:
722.4 (Digital Computers & Systems); 921.1 (Algebra)
722 (Computer Hardware); 921 (Applied Mathematics)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

17/5/3 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04760450 E.I. No: EIP97073734946
Title: Functional programming with graphs
Author: Erwig, Martin
Corporate Source: Fern Universitaet Hagen, Hagen, Ger
Conference Title: Proceedings of the 1997 ACM SIGPLAN International Conference on Functional Programming, ICFP
Conference Location: Amsterdam, Neth Conference Date: 19970609-19970611
Sponsor: ACM; SIGPLAN
E.I. Conference No.: 46625
Source: Proceedings of the ACM SIGPLAN International Conference on Functional Programming, ICFP 1997. ACM, New York, NY, USA. p 52-65
Publication Year: 1997
CODEN: 002374
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 9709W2
Abstract: Graph algorithms expressed in functional languages often suffer from their inherited imperative, state-based style. In particular, this impedes formal program manipulation. We show how to model **persistent graphs** in functional **languages** by graph constructors. This provides a decompositional view of graphs which is very close to that of data types and leads to a `more functional' formulation of graph algorithms. Graph constructors enable the definition of general fold operations for graphs. We present a promotion theorem for one of these folds that allows program fusion and the elimination of intermediate results. Fusion is not restricted to the elimination of tree-like structures, and we prove another theorem that facilitates the elimination of intermediate graphs. We

describe an ML-implement[redacted]on of persistent graphs which [redacted]iciently supports the presented fold operators. For example, depth-first-search expressed by a fold over a functional graph has the same complexity as the corresponding imperative algorithm. (**Author** abstract) 24 Refs.
Descriptors: *Computer programming; Graph theory; Algorithms; Theorem proving; Computer programming languages; Data structures; Program compilers ; Optimization; Computational complexity
Identifiers: Functional programming; Functional languages; Pattern matching
Classification Codes:
723.1.1 (Computer Programming Languages)
723.1 (Computer Programming); 921.4 (Combinatorial Mathematics, Includes Graph Theory, Set Theory); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory); 723.2 (Data Processing); 921.5 (Optimization Techniques)
723 (Computer Software); 921 (Applied Mathematics); 721 (Computer Circuits & Logic Elements)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

17/5/4 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04604522 E.I. No: EIP97013507738
Title: Adaptive control of robots by linear time-varying dynamic position feedback
Author: Lee, Ti-Chung; Chen, Bor-Sen; Chang, Yeong-Chan
Corporate Source: Natl Tsing-Hua Univ, Hsin Chu, Taiwan
Source: International Journal of Adaptive Control and Signal Processing v 10 n 6 Nov-Dec 1996. p 649-671
Publication Year: 1996
CODEN: IACPED ISSN: 0890-6327
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 9703W3
Abstract: A simple linear adaptive controller based on a reduced-order observer is proposed to treat the trajectory tracking control problem of robotic systems with unknown parameters and external disturbances. The novelty of our result lies in the fact that the controller is a linear time-varying dynamic position feedback compensator; the dimension of the observer, which is constructed only to estimate the velocity signal, is half the dimension of the robotic system and the attraction region of the closed-loop error system can not be only arbitrarily preassigned but also explicitly constructed. Moreover, as the adaptation is switched off, the boundedness of all the variables is still guaranteed and the trajectories of the closed-loop error **system** converge to any desired region. If the regressor **matrix** satisfies the **persistent** excitation condition, then our control algorithm also guarantees that the estimated values of the unknown parameters converge to the true ones. (**Author** abstract) 13 Refs.
Descriptors: *Robotics; Linear control systems; Adaptive control systems; Feedback; Closed loop control systems; Motion control; Time varying control systems; Manipulators; Algorithms
Identifiers: Closed loop error systems; Dynamic position feedback
Classification Codes:
731.5 (Robotics); 731.1 (Control Systems); 731.3 (Specific Variables Control); 691.1 (Materials Handling Equipment)
731 (Automatic Control Principles); 691 (Bulk Materials Handling); 921 (Applied Mathematics)
73 (CONTROL ENGINEERING); 69 (MATERIALS HANDLING); 92 (ENGINEERING MATHEMATICS)

17/5/5 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04127124 E.I. No: EIP95042650605

Title: Statistical [redacted]lysis of load behavior parame[redacted]s at four major loads
Author: Srinivasan, Krishnaswamy; Lafond, Claude
Corporate Source: IREQ, Varennes, Que, Can
Source: IEEE Transactions on Power Systems v 10 n 1 Feb 1995. p 387-392
Publication Year: 1995
CODEN: ITPSEG ISSN: 0885-8950
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications); G; (General Review)
Journal Announcement: 9506W1
Abstract: This paper describes field experience with a measurement system, which has been used to monitor the load behavior of four major loads at 230Kv level during the last 3 years. A statistical analysis of static load model parameters, estimated from 2768 snap shots of voltage perturbations is presented. Most of the perturbations are between 1% and 4%. However, 22 perturbations with voltage variations exceeding 20% have been recorded. The analysis of the same data to fit other more complex models will be discussed in a future paper. (**Author** abstract) 4 Refs.
Descriptors: *Electric loads; Electric power systems; Computer simulation ; Electric variables measurement; Statistical methods; Perturbation techniques; Stability; Electric utilities; Monitoring; Electric power supplies to apparatus
Identifiers: Power **system** simulation; Static load response parameters; High voltage signal interface; Substation **resident** unit; **Graphical** display
Classification Codes:
706.1 (Electric Power Systems); 723.5 (Computer Applications); 942.2 (Electric Variables Measurements); 922.2 (Mathematical Statistics)
706 (Electric Transmission & Distribution); 723 (Computer Software); 942 (Electrical & Electronic Measuring Instruments); 922 (Statistical Methods); 921 (Applied Mathematics)
70 (ELECTRICAL ENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 94 (INSTRUMENTS & MEASUREMENT); 92 (ENGINEERING MATHEMATICS)

17/5/6 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03976083 E.I. No: EIP94112410074
Title: Technique for the design of microprocessor memory systems
Author: Cupal, Jerry J.
Corporate Source: Univ of Wyoming, Laramie, WY, USA
Source: IEEE Transactions on Education v 37 n 3 Aug 1994. p 237-242
Publication Year: 1994
CODEN: IEEDAB ISSN: 0018-9359
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications)
Journal Announcement: 9412W4
Abstract: A systematic technique for the design of the chip select logic for microprocessor memory systems is given. In this technique, a memory table must be completed that shows the logic levels on each address line required to place every device (RAM, ROM, and I/O ports) at their desired locations **in memory** space. The memory **table** helps a designer visualize the **system** requirements and properly design the address decoding logic. The possibilities of bus contention can easily be recognized and avoided either by hardware or use of proper device locations in software. The technique is also a useful analysis tool. (**Author** abstract) 8 Refs.
Descriptors: *Data storage equipment; Microcomputers; Systems analysis; Microprocessor chips; Logic gates; Decision tables; Computer aided software engineering; Computer software; Computer aided analysis; Computer systems
Identifiers: Microprocessor memory systems; Chip select logic; Memory table; Logic levels
Classification Codes:
722.1 (Data Storage, Equipment & Techniques); 722.4 (Digital Computers & Systems); 714.2 (Semiconductor Devices & Integrated Circuits); 721.2

(Logic Elements); 723.5 (Computer Applications)
722 (Computer Hardware); 714 (Electronic Components); 721 (Computer Circuits & Logic Elements); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

17/5/7 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03629269 E.I. No: EIP93040764334
Title: Theoretical characteristics of a tunable two-electrode Fabry-Perot (TEFP) laser diode
Author: Le Bihan, Jean; Goujon, Jean-Marc; Auffret, Rene; Chawki, Mouhamad Jamil
Corporate Source: ENIB, Brest, Fr
Source: Journal of Lightwave Technology v 10 n 12 Dec 1992. p 1931-1934
Publication Year: 1992
CODEN: JLTEDG ISSN: 0733-8724
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 9307W1
Abstract: Tuning analysis of a two-electrode Fabry-Perot laser diode has been studied theoretically. Theoretical power and wavelength characteristics have been derived from an analytical model. This two-electrode Fabry-Perot laser presents a wide tuning range, which makes it able to operate in FM- and AM optical communication **systems** . (Author abstract) 10 Refs.
Descriptors: *Semiconductor lasers; Semiconductor diodes; Tuning; Optical communication equipment; Frequency modulation; Amplitude modulation
Identifiers: Fabry-Perot laser diodes; Laser diodes; Two-electrode laser diodes; Tunable laser diodes
Classification Codes:
744.4.1 (Semiconductor Lasers)
744.4 (Solid State Lasers); 714.2 (Semiconductor Devices & Integrated Circuits); 717.2 (Optical Communication Equipment); 741.3 (Optical Devices & Systems)
744 (Lasers); 714 (Electronic Components); 717 (Electro-Optical Communications); 741 (Optics & Optical Devices)
74 (OPTICAL TECHNOLOGY); 71 (ELECTRONICS & COMMUNICATIONS)

17/5/8 (Item 8 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03423032 E.I. Monthly No: EI9205064110
Title: Detection of persistent and transient defects in complex technical systems diagnosed by incomplete tests.
Author: Gorelov, O. I.
Corporate Source: Republican Scientific-Research Inst of Microinstruments, Riga, USSR
Source: Automation and Remote Control (English translation of Avtomatika i Telemekhanika) v 52 n 7 pt 2 Dec 20 1991 p 994-1002
Publication Year: 1991
CODEN: AURCAT ISSN: 0005-1179
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 9205
Abstract: We consider a structural mathematical model of complex technical systems in the form of diagnostic graphs. A general approach is developed to the analysis of arbitrary diagnostic **graphs** for computing suspected **persistent** and transient defects in components and connections in such **systems** . (**Author** abstract) 7 Refs.
Descriptors: *LOGIC CIRCUITS, COMBINATORIAL--*Automatic Testing; COMPUTERS, DIGITAL--Shift Registers
Identifiers: TEST **GENERATORS** ; LINEAR FEEDBACK SHIFT REGISTERS
Classification Codes:

721 (Computer Circuit[redacted] Logic Elements); 722 (Comput[redacted]ardware)
72 (COMPUTERS & DATA PROCESSING)

17/5/9 (Item 9 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02659850 E.I. Monthly No: EIM8810-053583
Title: SOFTWARE PACKAGE FOR THE ANALYSIS OF GENERAL MULTILAYER PERFORMANCE DATA.
Author: Peterson, Bryan G.; Pew, Hans K.; Knight, Larry V.; Gaines, David P.
Corporate Source: Brigham Young Univ, Provo, UT, USA
Conference Title: Soft X-Ray Optics and Technology.
Conference Location: Berlin, West Ger Conference Date: 19861208
Sponsor: Berliner Elektronenspeicherring-Gesellschaft fuer Synchrotronstr ahlung mbH, Berlin, West Ger; SPIE, Bellingham, WA, USA; Fritz-Haber-Inst der Max-Planck-Gesellschaft, Berlin, West Ger; Brookhaven Natl Lab/Natl Synchrotron Light Source, USA
E.I. Conference No.: 11601
Source: Proceedings of SPIE - The International Society for Optical Engineering v 733. Publ by SPIE, Bellingham, WA, USA p 405-409
Publication Year: 1987
CODEN: PSISDG ISSN: 0277-786X ISBN: 0-89252-768-4
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8810
Abstract: In an effort to make data on the reflectivity and transmission of multilayer optical elements more usable, we have developed a computer code for the manipulation and graphical display of a general data set consisting of x, y, and delta-y values. The code was developed for a DEC VAX computer running a version 4. 2 or later VMS operating system. Facilities are available for algebraic manipulation, editing, smoothing, interpolating, and deconvolving data sets in a straightforward way. The code is entirely self-contained with the exception of the graphics output support, which is centralized to allow for simple interfacing to the **graphics** package **resident** on the target **system** . The capabilities of the code are described and sample output is shown. (**Author** abstract) 6 refs.
Descriptors: *OPTICAL SYSTEMS--*Computer Aided Analysis; X-RAYS
Identifiers: MULTILAYER PERFORMANCE; COMPUTER CODE; LINE PLOT **GENERATION**
Classification Codes:
741 (Optics & Optical Devices); 941 (Acoustical & Optical Measuring Instruments); 723 (Computer Software); 932 (High Energy, Nuclear & Plasma Physics)
74 (OPTICAL TECHNOLOGY); 94 (INSTRUMENTS & MEASUREMENT); 72 (COMPUTERS & DATA PROCESSING); 93 (ENGINEERING PHYSICS)

17/5/10 (Item 10 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02034328 E.I. Monthly No: EI8610093975 E.I. Yearly No: EI86023164
Title: INTEGRATED GRAPHICS PROGRAMMING ENVIRONMENT.
Author: Morrison, R.; Florianis, A. L.; Dearle, A.; Atkinson, M. P.
Corporate Source: Univ of St. Andrews, St. Andrews, Scotl
Source: Computer Graphics Forum v 5 n 2 Jun 1986, EUROGRAPHICS (UK) Conf, Glasgow, Scotl, Mar 26-28 1986 p 147-157
Publication Year: 1986
CODEN: CGFODY ISSN: 0167-7055
Language: ENGLISH
Document Type: JA; (Journal Article) Treatment: A; (Applications); M; (Management Aspects)
Journal Announcement: 8610
Abstract: The facilities of the PS-algol programming language are described in this paper to show how they may be used to provide an

integrated **graphics** programming environment. The **persistent** store mechanism and the secure transaction facilities of the **language** provide the basic environment in which an integrated system may be implemented. This is augmented by data types and operations to support line drawings and raster graphics. The combination of these mechanisms may be used to provide the integrated graphics programming environment. (**Author** abstract) 15 refs.
Descriptors: *COMPUTER PROGRAMMING LANGUAGES--*ALGOL; COMPUTER GRAPHICS; DATABASE SYSTEMS--Management
Identifiers: PERSISTENT STORE; LINE DRAWINGS; RASTER GRAPHICS; PICTURE LIBRARIES; PS-ALGOL
Classification Codes:
723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

17/5/11 (Item 11 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01938758 E.I. Monthly No: EI8601001364 E.I. Yearly No: EI86023227
Title: TLC-LISP.
Author: WONG, WILLIAM G.
Corporate Source: LOGIC FUSION INC, YARDLEY, PA, USA
Source: BYTE V 10 N 10 OCT 1985 P 287-288, 290, 292
Publication Year: 1985
CODEN: BYTEDJ ISSN: 0360-5280
Language: ENGLISH
Document Type: JA; (JOURNAL ARTICLE)
Journal Announcement: 8601
Abstract: TLC-LISP IS AN IMPLEMENTATION OF LISP FOR 8086/8088-BASED MACHINES RUNNING PC-DOS, MS-DOS, CP/M-86, OR CONCURRENT DOS. IT CAN USE ALL AVAILABLE MEMORY UP TO 1 MEGABYTE AND SUPPORTS THE 8087 NUMERIC COPROCESSOR. A **RESIDENT** SCREEN EDITOR, TURTLE- **GRAPHICS** SUPPORT, A SMALLTALK-LIKE CLASS **SYSTEM** , AND A LISP MACHINE-LIKE PACKAGE SYSTEM MAKE TLC-LISP AN ATTRACTIVE **ALTERNATIVE** FOR ARTIFICIAL INTELLIGENCE (AI) WORK. (**AUTHOR** ABSTRACT)
Descriptors: *COMPUTER PROGRAMMING LANGUAGES--*LISP; COMPUTER OPERATING SYSTEMS--PROGRAM COMPILERS; DATA STORAGE, MAGNETIC--DISK; COMPUTER GRAPHICS --INTERACTIVE; ARTIFICIAL INTELLIGENCE
Identifiers: TLC-LISP; RESIDENT SCREEN EDITOR; TURTLE-GRAPHICS SUPPORT
Classification Codes:
723 (Computer Software); 722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING)

17/5/12 (Item 12 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01800832 E.I. Monthly No: EI8509076508 E.I. Yearly No: EI85029220
Title: METHOD TO CREATE AND ACTIVATE PROFILE FUNCTIONS FOR MULTIPLE-USER PROFILES.
Author: Anon
Source: IBM Technical Disclosure Bulletin v 28 n 2 Jul 1985 p 787-789
Publication Year: 1985
CODEN: IBMTAA ISSN: 0018-8689
Language: ENGLISH
Document Type: JA; (Journal Article) Treatment: A; (Applications)
Journal Announcement: 8509
Abstract: A method is described which allows the **creation** of user profiles as a single DOS file rather than proliferating DOS files for each machine function requiring profile information. The term 'user-defined profile' refers to a DOS flat file dataset that contains unique system hardware and text defaults that are customized/tailored by the user. The 'system profile' which contains the system default hardware and text characteristics of the program is always loaded during IPL by default. It is desirable in many instances to have defaults loaded at IPL (initial

program load) that are different from the system profile (default). The method for loading a user-defined profile at IPL reads the user profile dataset tables into the memory location of the system profile tables and overlays the **system** profile tables with the user profile **tables in RAM** (random-access memory). The DOS file name associated with the user profile dataset is an input parameter supplied to the initialization command in order to activate the file.
Descriptors: *DATA PROCESSING--*File Organization; DATABASE SYSTEMS
Identifiers: PROFILE FUNCTIONS; MULTIPLE-USER PROFILES; DOS FLAT FILE; IPL (INITIAL PROGRAM LOAD)
Classification Codes:
723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

17/5/13 (Item 13 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

00908028 E.I. Monthly No: EI8004027831 E.I. Yearly No: EI80015644
Title: EXPERIENCE IN MEASURING AND TUNING THE OPERATING SYSTEMS **OF COMPUTERS.**
Author: Vinnichenko, A. I.; Gurin, N. N.; Kogan, Ya. A.; Lyapicheva, N. G.
Source: Programming and Computer Software (English Translation of Programmirovanie) v 5 n 1 Jan-Feb 1979 p 49-57
Publication Year: 1979
CODEN: PCSODA
Language: ENGLISH
Journal Announcement: 8004
Abstract: The method is described of carrying out measurements and tuning of computer operating **systems** . Two problems are considered: the definition of the composition of **resident** modules and **tables** of the OS and the selection of a rational disposition of **system** data sets on direct access devices (DAD). For the solution of these problems, a record was kept of **parameters** of **accesses** to DAD in the course of the OS functioning. 7 refs.
Descriptors: COMPUTER OPERATING **SYSTEMS**
Classification Codes:
723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

17/5/14 (Item 14 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

00817431 E.I. Monthly No: EI7905032509 E.I. Yearly No: EI79026828
Title: PRACTICAL IMPLEMENTATION ON A 5 kVA SYNCHRONOUS GENERATOR **OF AN ADAPTIVE EXCITATION CONTROLLER STRATEGY FOR A WIDE RANGE OF OPERATING CONDITIONS.**
Author: Phung, V. A.; Gibbard, M. J.
Corporate Source: Univ of Adelaide, South Aust
Source: Proceedings of the Institution of Electrical Engineers (London) v 125 n 10 Oct 1978 p 1009-1020
Publication Year: 1978
CODEN: PIEEAH ISSN: 0020-3270
Language: ENGLISH
Journal Announcement: 7905
Abstract: The feasibility of implementing an adaptive-control strategy to the excitation of a synchronous **generator** was examined in the laboratory. The aim of this work, which extends previous investigations based on an optimal-control strategy, is to design a practical controller that is not only suitable for continuous operation, but also meets tight steady-state and dynamic performance criteria over a wide range of leading power-factor steady-state operating conditions. Optimal-control theory is used as a means of determining 'off-line' the required feedback gains, use being made of a linearized model of the system for specific operating conditions. A

minicomputer which acts [redacted]he real-time controller, esti[redacted]es the 'pseudo' steady-state operating point at any instant and selects the appropriate feedback gains from a 'look-up' **table** stored **in** **memory** . The experimental **system** is tested for a wide range of disturbances of a significant magnitude, and the results compared with predicted responses based on a non-linear machine model. 11 refs.

Descriptors: ELECTRIC **GENERATORS** , SYNCHRONOUS--*Design; CONTROL SYSTEMS, OPTIMAL; CONTROL SYSTEMS, ADAPTIVE

Classification Codes:

705 (Electric Generators & Motors); 731 (Automatic Control Principles); 732 (Control Devices)

70 (ELECTRICAL ENGINEERING); 73 (CONTROL ENGINEERING)

17/5/15 (Item 15 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

00476528 E.I. Monthly No: EI7509062595 E.I. Yearly No: EI75073251

Title: Covering Peak Loads by Supplementary Increase of the Capacities of 150 and 200 MW Power Units.

Title: POKRYTIE PIKOVYKH NAGRUZOK DOPOLNITEL'NYM UVELICHENIEM MOSHCHNOSTI ENERGOBLOKOV 150, 200 MVt.

Author: Dikmarov, S. V.; Bilyk, N. S.; Tret'yakova, L. I.

Corporate Source: L'vov Polytech Inst, Ukr SSR

Source: Izvestiya Vysshikh Uchebnykh Zavedenii, Energetika n 4 Apr 1975 p 3-8

Publication Year: 1975

CODEN: IVZEAY ISSN: 0579-2983

Language: RUSSIAN

Journal Announcement: 7509

Abstract: The advantages of the replacement of feed electric pumps (FEP) in 150, 200 mw power units by turboelectric feed pumps (**TEFP**) consisting of a feed pump (FP), a synchronous motor (SM), a turbine with counterpressure and two steam bleedings (ST) with the capacity equal to the capacity of the FP and SM, are investigated. Conditions of operation of 150, 200 MW power units with disconnected high pressure heaters (HPH) and utilization of the bled and counterpressure steam of the ST in the HPH of the main turbines are considered. Using the example of the Lvov power **system** , the performance and efficiency indices of covering the peak load by the released capacity of 150, 200 MW power units with disconnected HPH and connected **TEFP** and gas turbine plant are compared. In Russian.

Descriptors: *STEAM POWER PLANTS--*Standby Service

Classification Codes:

614 (Steam Power Plants)

61 (PLANT & POWER ENGINEERING)

17/5/16 (Item 1 from file: 35)

DIALOG(R)File 35:Dissertation Abs Online

01164664 ORDER NO: AAD91-19879

A PERSISTENT ENVIRONMENT FOR MICRO-INCREMENTAL REUSE (SOFTWARE REUSE, VERSION MANAGEMENT)

Author: KAZEROONI-ZAND, MANSOUR

Degree: PH.D.

Year: 1990

Corporate Source/Institution: OKLAHOMA STATE UNIVERSITY (0664)

Source: VOLUME 52/02-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 933. 163 PAGES

Descriptors: COMPUTER SCIENCE

Descriptor Codes: 0984

Scope and method. Software engineers/programmers are constantly called upon to produce more and more software, and their productivity continues to be an increasingly pressing problem. Recent surveys and papers on reusability of software strongly indicated that software reuse is a major

way to boost software engineering productivity. The main objective of this dissertation is to present a new approach to the reuse of existing software, called ROPCO. Reuse On Persistent Code and Object-code is an integrated collection of techniques, tools, and structures to facilitate the reusability of persistent code and object-code. To make code and object-code level a feasible **alternative** as a reuse level, three main issues are addressed as the prime objectives in the design of software development environments: locating segment of code and object code, **modification** and recompilation of code, and persistency and version management. The issues of what is the unit of reuse and how these units can be put together are also addressed in this study.

Finding and conclusions. To meet the design goals, ROPCO is designed in three layers: IDentification Mechanism (IDM), Software Control Mechanism (SCM), and Interface. Templates and modules are selected for the unit of reuse, and a template is used as the unit of persistency. As the kernel of ROPCO, SCM is an integrated collection of techniques and structures to preform the task of persistency and version management, as well as **modification** and coordinating of the recompilation tasks. SCM utilizes new ideas such as **Persistent** network and symbol **table** , a **persistent** hierarchical structure, and a module/template interconnection **language** . Incorporation of these new concepts, plus enhanced recompilation techniques, into the design of the ROPCO environment provide the necessary capabilities for such an environment. However, to amplify ROPCO's capabilities some of the concepts utilized in Domain Analysis, Reengineering, Reverse Engineering needs to be incorporated in the design of the revised version of ROPCO.

17/5/17 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6398630 INSPEC Abstract Number: A1999-24-4281P-007, B1999-12-7230E-025
Title: A study on the development of transmission-type extrinsic Fabry-Perot interferometric optical fiber sensor
Author(s): Sang-Hoon Kim; Jung-Ju Lee; Dong-Chun Lee; Il-Bum Kwon
Author Affiliation: Dept. of Mech. Eng., Korea Adv. Inst. of Sci. & Technol., Seoul, South Korea
Journal: Journal of Lightwave Technology vol.17, no.10 p.1869-74
Publisher: IEEE,
Publication Date: Oct. 1999 Country of Publication: USA
CODEN: JLTEDG ISSN: 0733-8724
SICI: 0733-8724(199910)17:10L.1869:SDTT;1-J
Material Identity Number: E771-1999-011
U.S. Copyright Clearance Center Code: 0733-8724/99/$10.00
Document Number: S0733-8724(99)07997-9
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Theoretical (T)
Abstract: The conventional reflection-type extrinsic Fabry-Perot interferometric (EFPI) optical fiber sensor has good sensitivity and resolution compared with other types of optical fiber sensors. However, they have the disadvantage that the distinction of strain direction of EFPI is difficult because of measurement method by only fringe counting. This paper presents the newly developed transmission-type EFPI (**TEFPI**) optical fiber sensor, which has been improved by additional functions, and whose measuring **system** differs from that of the reflection-type EFPI optical fiber sensors using a single-mode fiber (SMF) and multimode (MMF) fibers as light guides and reflectors, respectively. The output signal of the **TEFPI** optical fiber sensor was analyzed with the uniform plane wave-based model, the SMF power distribution-based model and the splice loss-based model; the analyzed signals were then verified experimentally. Based on the results of analysis, the **TEFPI** optical fiber sensor was fabricated using two single-mode fibers connected to the light source and optical receiver; this was then used in strain measurement. The strain measured by the **TEFPI** optical fiber sensor was compared with that measured by the electric strain gauge. (16 Refs)
Subfile: A B
Descriptors: Fabry-Perot interferometers; fibre optic sensors;

reflectivity; strain sen[redacted]s
Identifiers: transmission-type extrinsic Fabry-Perot interferometric optical fiber sensor; reflection-type extrinsic Fabry-Perot interferometric optical fiber sensor; good sensitivity; resolution; strain direction; fringe counting; measuring **system** ; single-mode fiber; multimode fibers; light guides; uniform plane wave-based model; distribution-based model; splice loss-based model; optical receiver; strain measurement; strain sensors
Class Codes: A4281P (Fibre optic sensors; fibre gyros); A0760L (Optical interferometry); A0630M (Measurement of mechanical variables); A0670D (Sensing and detecting devices); B7230E (Fibre optic sensors); B7320G (Mechanical variables measurement)

17/5/18 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5511905 INSPEC Abstract Number: C9704-7120-025
Title: The OMG Events Service
Author(s): Schmidt, D.C.; Vinoski, S.
Journal: C++ Report vol.9, no.2 p.37-46
Publisher: SIGS Publications,
Publication Date: Feb. 1997 Country of Publication: USA
CODEN: CRPTE7 ISSN: 1040-6042
SICI: 1040-6042(199702)9:2L.37:ES;1-P
Material Identity Number: O697-97002
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: The authors previously **modified** their stock quote system to implement distributed callbacks using CORBA. The problems with the notifying stock quoter can be eased somewhat if one separates concerns. In particular, the Supplier's Notifying Quoter implementation has enough to worry about within its own problem domain as it monitors and reports changing stock values. Therefore, one should avoid making it also responsible for delivering notifications to multiple consumers, handling blocking caused by network congestion and end **system** load, and maintaining a **persistent table** of callbacks. All these tasks are independent of the stock quoter application domain. One way to relieve some of the burden placed on the stock quoter is to utilize an implementation of the OMG Events Service to deliver notifications. The Events Service is one component in the OMG Common Object Services Specification (COSS) Volume 1.2. Its purpose is to provide delivery of event data from suppliers to consumers without requiring these participants to know about each other explicitly. Therefore, implementations of the Events Service act as mediators that support decoupled communication between objects. (0 Refs)
Subfile: C
Descriptors: client-server systems; financial data processing; object-oriented methods; object-oriented programming; stock markets
Identifiers: OMG Events Service; notifying stock quoter; changing stock values; OMG Common Object Services Specification Volume 1.2; event data delivery; suppliers; consumers; inter-object decoupled communication
Class Codes: C7120 (Financial computing); C6110J (Object-oriented programming); C6110F (Formal methods); C6150N (Distributed systems software)

17/5/19 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

5387532 INSPEC Abstract Number: A9622-6170G-003
Title: Stochastic dislocation patterning during cyclic plastic deformation. A theory of the formation **of** persistent **slip band and** matrix **structures**
Author(s): Haehner, P.

Author Affiliation: [redacted]nt Res. Centre, Comm. of the [redacted]r. Communities, Ispra, Italy
Journal: Applied Physics A (Materials Science Processing) vol.63, no.1 p.45-55
Publisher: Springer-Verlag,
Publication Date: July 1996 Country of Publication: Germany
CODEN: APAMFC ISSN: 0947-8396
SICI: 0947-8396(199607)63:1L.45:SDPD;1-K
Material Identity Number: D218-96008
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: A dislocation dynamical theory is developed for the formation of dipole dislocation patterns during cyclic plastic deformation in single glide. The stochastic dislocation dynamics adopted is suitable to account, in terms of a fluctuating effective medium, for the effects of long-range dislocation interactions on a mesoscopic scale. The theory can explain the occurrence of a matrix structure and persistent slip bands as a result of evolutionary processes, it gives the intrinsic strain amplitudes and the characteristic wavelength of these structures, and it allows for an interpretation of the structural **changes** associated with **changes** of the deformation conditions. Quantitative results are in good agreement with experimental observations. (39 Refs)
Subfile: A
Descriptors: digital simulation; dislocation dipoles; dislocations; fatigue; Fokker-Planck equation; plastic deformation; stochastic processes; stress-strain relations; work hardening
Identifiers: stochastic dislocation patterning; cyclic plastic deformation; slip band structure; matrix structure; dislocation dynamical theory; dipole dislocation patterns; long range interactions; dislocation interactions; mesoscopic scale; intrinsic strain amplitudes; stress strain relations; Fokker Planck equation; work hardening; temperature dependence; 77 to 300 K
Class Codes: A6170G (Dislocations: theory); A6170L (Slip, creep, internal friction and other indirect evidence of dislocations); A6220F (Deformation and plasticity); A4630J (Viscoelasticity, plasticity, viscoplasticity, creep, and stress relaxation)
Numerical Indexing: temperature 7.7E+01 to 3.0E+02 K

17/5/20 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

04329574 INSPEC Abstract Number: B9303-6430C-007
Title: Picture conversion for high-definition graphics
Author(s): Pank, R.A.
Author Affiliation: Quantel Ltd., Newbury, UK
Journal: SMPTE Journal vol.101, no.11 p.797-9
Publication Date: Nov. 1992 Country of Publication: USA
CODEN: SMPJDF ISSN: 0036-1682
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: In the high-definition (HD) production environment the use of 1125/60 and 1250/50 formats **creates** the need for conversion at the HD level, while down and upconversions to the established 525/60 and 625/50 broadcast systems are also required. In the particular case of stills used in **graphics systems** , their existing **resident** facilities can be employed to provide high-quality conversions automatically. In this way images may be passed between systems for use in the different HD and broadcast standards. In addition, graphic elements may be successfully sourced from any format to make a composite image. Such techniques have an obvious long-term application as well as helping users to negotiate the current HD standards 'minefield'. (0 Refs)
Subfile: B
Descriptors: high definition television; television production; television standards
Identifiers: high definition production; picture conversion; high

definition standards; aspect ratio; high-definition graphics; broadcast systems; graphics systems; broadcast standards; composite image
Class Codes: B6430C (High definition television); B6420 (Radio and television broadcasting)

17/5/21 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

04094783
Title: Clock in trade (Timeslips III)
Author(s): Sedacca, B.
Journal: Personal Computer Magazine p.63
Publication Date: Jan. 1992 Country of Publication: UK
CODEN: PECME7
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Product Review (R)
Abstract: Timeslips III tracks time and expenses of tasks performed for a particular client at a specific rate. From this information, a variety of reports can be **generated** , from itemised invoices to account history and staff performance analyses. The **system** can **create** over 40 macros and over 30 types of **graphs** . A memory **resident** timer module allows users to log a time record to the system at any time without leaving their application. A stopwatch timer can be activated for any activity, and when the time record is completed, the client's file automatically updated. Automatic payment from client funds account can be made to cover time and/or expenses charges. Each client can have a custom billing format. (0 Refs)
Subfile: D
Descriptors: accounting; marketing; software packages
Identifiers: time tracking; expense tracking; Timeslips III; account history; staff performance analyses; custom billing
Class Codes: D2050B (Accounting); D2140 (Marketing, retailing and distribution)

17/5/22 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

03082162 INSPEC Abstract Number: A88031804, C88020389
Title: A software package for the analysis of general multilayer performance data
Author(s): Peterson, B.G.; Pew, H.K.; Knight, L.V.; Gaines, D.P.
Author Affiliation: Dept. of Phys. & Chem., Brigham Young Univ., Provo, UT, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering vol.733 p.405-9
Publication Date: 1987 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
Conference Title: Soft X-Ray Optics and Technology
Conference Sponsor: SPIE: Berliner Elektronenspeicherring-Gesellschaft Synchrotronstrahlung
Conference Date: 8-11 Dec. 1986 Conference Location: Berlin, West Germany
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Experimental (X)
Abstract: In an effort to make data on the reflectivity and transmission of multilayer optical elements more usable, the authors have developed a computer code for the manipulation and graphical display of a general data set consisting of x, y, and delta-y values. The code was developed for a DEC VAX computer running a version 4.2 or later VMS operating system. Facilities are available for algebraic manipulation, editing, smoothing, interpolating, and deconvolving data sets in a straightforward way. The code is entirely self-contained with the exception of the graphics output support, which is centralized to allow for simple interfacing to the

graphics package **res[illegible]nt** on the target **system** . Th[illegible]apabilities of the code are described and sample output is shown. (6 Refs)

Subfile: A C

Descriptors: light transmission; mirrors; optical design techniques; optical films; optical systems; physics computing; reflectivity; software packages; superlattices; X-ray apparatus

Identifiers: data manipulation; mirrors; line plot **generation** ; soft X-ray region; software package; general multilayer performance data; reflectivity; transmission; multilayer optical elements; computer code; graphical display; DEC VAX computer; algebraic manipulation; editing; smoothing; interpolating; deconvolving

Class Codes: A0650D (Data gathering, processing, and recording, data displays including digital techniques); A0785 (X-ray, gamma-ray instruments and techniques); A4278C (Lens and mirror design); A4278D (Optical system design); A4278H (Coatings); C7320 (Physics and Chemistry)

17/5/23 (Item 7 from file: 2)

DIALOG(R)File 2:INSPEC

01293998 INSPEC Abstract Number: B79006757, C79005003

Title: Practical implementation on a 5 kVA synchronous generator **of an adaptive excitation controller strategy for a wide range of operating conditions**

Author(s): Phung, V.A.; Gibbard, M.J.

Author Affiliation: Dept. of Electrical Engng., Univ. of Adelaide, Adelaide, SA, Australia

Journal: Proceedings of the Institution of Electrical Engineers vol.125, no.10 p.1009-14

Publication Date: Oct. 1978 Country of Publication: UK

CODEN: PIEEAH ISSN: 0020-3270

Language: English Document Type: Journal Paper (JP)

Treatment: Applications (A); Practical (P); Experimental (X)

Abstract: The feasibility of implementing an adaptive-control strategy to the excitation of a synchronous **generator** has been examined in the laboratory with the aim to design a practical controller that is not only suitable for continuous operation, but also meets tight steady-state and dynamic performance criteria over a wide range of leading power-factor steady-state operating conditions. Optimal-control theory is used as a means of determining 'off-line' the required feedback gains, use being made of a linearised model of the system for specific operating conditions. A minicomputer, which acts as the real-time controller, estimates the 'pseudo' steady-state operating point at any instant and selects the appropriate feedback gains from a 'look-up' **table** stored **in memory** . The experimental **system** is tested for a wide range of disturbances of a significant magnitude, and the results compared with predicted responses based on a nonlinear machine model. Good agreement is obtained, and performance criteria are achieved. (11 Refs)

Subfile: B C

Descriptors: adaptive control; controllers; exciters; optimal control; power system computer control; synchronous **generators**

Identifiers: 5 kVA; synchronous **generator** ; adaptive excitation controller; optimal control; real time controller; power system computer control

Class Codes: B8310D (Synchronous machines); B8380 (Control gear and apparatus); C1330 (Optimal control); C1340E (Self-adjusting systems); C3340H (Electric systems); C7410B (Power engineering)

17/5/24 (Item 1 from file: 94)

DIALOG(R)File 94:JICST-EPlus

03089057 JICST ACCESSION NUMBER: 97A0183717 FILE SEGMENT: JICST-E

Streetscape Simulation System **for** Residential **Area Employing Computer** Graphics .

SUGIYAMA TAKEMI (1); AIBA YASUO (1)

(1) Tohoku Univ. Art & Design
Joho, Shisutemu, Riyo, Gijutsu Shinpojiumu Ronbunshu(Proceedings of the Symposium on Computer Technology of Information, Systems and Applications), 1996, VOL.19th, PAGE.109-114, FIG.11, TBL.6, REF.2
JOURNAL NUMBER: S0463BBF
UNIVERSAL DECIMAL CLASSIFICATION: 712.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: In the field of townscape study, computer graphics have been frequently used as a means to provide visual material. Application of CG enables new ways of studying townscape. Among these applications, evaluation and comparison of the built environments with CG images is widely accepted because CG can provide images with certain credibility relatively easily. However, the image production has been employed only as visualization of either existing or some arbitrarily chosen conditions, and is not engaged in the process of simulation which determines the coming situation from existing conditions. This study, which is based on our past research in Yamagata city concerning the relation between the elements affecting streetscape and the site conditions, is to propose a simulation system which forecasts and visualizes streetscape of residential area from the site conditions. The system is made of two parts: one is a calculation part which determines size, shape and location of the elements from the site conditions and the other is an image production part which **creates** three-dimensional shapes and renders them with suitable texture and color. The calculation part is based on our past research in which 503 sites in residential area of Yamagata city were examined in terms of streetscape. The anlaysis of the research indicates that the elements comprising streetscape can be classified into two categories. One group is related with physical aspects of the site. Becuase of common requirements for the house such as having sunlight into the house and garden, ensuring privacy and access to the house, there exists a rule between some elements and the site conditions. The other group is not related to the site conditions and determined from owner's or architect's taste, financial ability, and interest to streetscape. The calculation process utilizes this division. Many elements have loose connection with the site conditions. (**author** abst.)
DESCRIPTORS: urban design; computer graphics; townscape; Yamagata; computer application system; housing land; street; simulation; image processing; residential district
BROADER DESCRIPTORS: design; image technology; technology; computer application; utilization; landscape; Tohoku District; Japan; East Asia; Asia; system; lot(land); road; information processing; treatment; district
CLASSIFICATION CODE(S): RD04010N

17/5/25 (Item 1 from file: 233)
DIALOG(R)File 233:Internet & Personal Comp. Abs.

00468670 97MH08-001
Musicians & the Mac -- Yeah, we love our Macs. And so do today's most innovative music artists! You're in good company. See why these professionals....
Shepherd, Carrie
MacHome Journal , August 1, 1997 , v5 n8 p20-23, 4 Page(s)
ISSN: 1074-0392
Languages: English
Document Type: Articles, News & Columns
Geographic Location: United States
Discusses the ways in which several professional musicians use the Macintosh as a **creativity** and development tool. Spotlights Thomas Dolby, who uses a Macintosh 8500 for business applications as well as composing and editing musical arrangements; Herbie Hancock, who uses a collection of high-end Macintosh **systems** for producing music and related **graphics** ;

The **Residents** , who pre[redacted] the Macintosh's multimedia cap[redacted]lities for the **creation** of their experimental music; and Brian Lies[redacted]ang of the band Filter, who prefers to program and record all the band's music on a Macintosh system. Also discusses how musicians utilize the Internet. Includes six photos. (kgh)

Descriptors: Music; Macintosh; Audio Processing; Internet; Case Study; Multimedia; Productivity Software

17/5/26 (Item 1 from file: 6)

DIALOG(R)File 6:NTIS

2003431 NTIS Accession Number: DE97003409

Measurements for the JASPER Program Flux Monitor Experiment

Muckenthaler, F. J. ; Spencer, R. R. ; Hunter, H. T. ; Hull, J. L. ; Shono, A.

Oak Ridge National Lab., TN.

Corp. Source Codes: 021310000; 4832000

Sponsor: Department of Energy, Washington, DC.

Report No.: ORNL/TM-12171

Feb 93 70p

Languages: English

Journal Announcement: GRAI9714; ERA9725

Sponsored by Department of Energy, Washington, DC.

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NTIS Prices: PC A05/MF A01

Country of Publication: United States

Contract No.: AC05-84OR21400

The Flux Monitor Experiment was conducted at the Oak Ridge National Laboratory (ORNL) Tower Shielding Facility (TSF) during the months of May and June 1992, as part of the continuing series of eight experiments planned for the Japanese-American Shielding Program for Experimental Research (JASPER) program that was started in 1986. This series of experiments was designed to examine shielding concerns and radiation transport effects pertaining to in-vessel flux monitoring systems (FMS) in current reactor shield designs proposed for both the Advanced Liquid Metal Reactor (ALMR) design and the Japanese loop-type design. The program is a cooperative effort between the United States Department of Energy (US DOE) and the Japanese Power Reactor and Nuclear Fuel Development Corporation (PNC). The Tower Shielding Reactor H (TSR-II) neutron source was **altered** by the spectrum **modifier** (SM) used previously in the Axial Shield Experiment, and part of the Japanese Removable Radial Shield (RRS) before reaching the axial shield. In the axial shield were placed six homogeneous boron carbide (B(sub 4)C) hexagons around a center hexagon of aluminum used to represent sodium. Shield designs to be studied were placed beyond the axial shield, each design forming a void directly behind the axial shield. Measurements were made in the void and behind each slab as successive slabs were added.

Descriptors: LMFBR Type Reactors; *Neutron Flux; Aluminium; Boron Carbides; Coordinated Research Programs; Design; Experimental Data; Japan; Monitoring; Radiation Transport; Reactor Monitoring **Systems** ; Shielding; Shielding Materials; **TSR** -2 Reactor; USA; **Tables** (data)

Identifiers: EDB/210500; EDB/220600; NTISDE

Section Headings: 77H (Nuclear Science and Technology--Reactor Engineering and Nuclear Power Plants); 77K (Nuclear Science and Technology--Reactor Physics)

17/5/27 (Item 2 from file: 6)

DIALOG(R)File 6:NTIS

1183159 NTIS Accession Number: AD-A154 966/6

Realizing the Full Potential of the Video Disc for Mapping Applications

Lambert, R. B.
Army Engineer Topographic Labs., Fort Belvoir, VA.
Corp. Source Codes: 008093000; 403192
Report No.: ETL-R-071
Mar 85 9p
Languages: English
Journal Announcement: GRAI8518
Presented at the ASP-ACSM Convention, 10-15 Mar 85, Washington, DC.
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A02/MF A01
Country of Publication: United States
Today, scientists at the US Army Engineer Topographic Laboratories (ETL) are investigating mapping applications of optical storage technology. Research efforts at ETL over the last several years have shown that a great potential exists for interactive optical video disc **systems** in storing and displaying maps, photographs and other **graphic** materials. ETL's **resident** demonstration video disc **system** has served well but cannot be easily adapted to new mapping aplications. A new system being developed at ETL uses state-of-the-art Direct Read After Write (DRAW) video disc technology for in-house recording of video discs. ETL's hybrid approach to data storage brings analog and digital mapping data together for the first time on the same video disc. Planning and production operations for video discs are being streamlined and cartographic standards are being developed to improve the quality of video map displays. (**Author**)
Descriptors: *Maps; *Optical storage; Data bases; Data storage systems; Digital maps; Digital systems; Disk recording systems; Disks; Graphics; Hybrid systems; Mapping; State of the art; Video recording
Identifiers: Video disks; NTISDODXA
Section Headings: 48I (Natural Resources and Earth Sciences--Cartography) ; 82C (Photography and Recording Devices--Recording Devices)

17/5/28 (Item 3 from file: 6)
DIALOG(R)File 6:NTIS

0996108 NTIS Accession Number: PB83-126490
Residential Detector Performance (Dollar Loss) - 1980
Fire Administration, Washington, DC.
Corp. Source Codes: 058935000
24 Mar 82 299p
Languages: English
Journal Announcement: GRAI8304
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A13/MF A01
Country of Publication: United States
This document contains computer tables **generated** from data collected by the NFIRS for use as supportive data only and requires understanding and familiarity of the data system.
Descriptors: Fires; *Statistical data; * **Residential** buildings; **Tables** (Data); Fire detection **systems** ; Fire damage; Losses
Identifiers: NTISFEMFDC
Section Headings: 89H (Building Industry Technology--Building Equipment, Furnishings, and Maintenance)

17/5/29 (Item 4 from file: 6)
DIALOG(R)File 6:NTIS

0995828 NTIS Accession Number: PB83-122614
Residential Detector Performance (Civilian Deaths) - 1980

Federal Emergency Management Agency, Washington, DC.
Corp. Source Codes: 057043000
23 Mar 82 303p
Languages: English
Journal Announcement: GRAI8304
See also report for 1979, PB83-118703.
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A14/MF A01
Country of Publication: United States
This document contains computer tables **generated** from data collected by the NFIRS for use as supportive data only and requires understanding and familiarity of the data system.
Descriptors: Fires; *Statistical data; * **Residential** buildings; **Tables** (Data); Fire detection **systems** ; Evaluation; Casualties; Death
Identifiers: Accident causes; NTISFEMFDC
Section Headings: 89H (Building Industry Technology--Building Equipment, Furnishings, and Maintenance)

17/5/30 (Item 5 from file: 6)
DIALOG(R)File 6:NTIS

0995627 NTIS Accession Number: PB83-119107
Residential Detector Performance (Civilian Injuries 1979)
Federal Emergency Management Agency, Washington, DC.
Corp. Source Codes: 057043000
26 Sep 80 277p
Languages: English
Journal Announcement: GRAI8304
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A13/MF A01
Country of Publication: United States
This document contains computer tables **generated** from data collected by the NFIRS for use as supportive data only and requires understanding and familiarity of the data system.
Descriptors: Fires; *Statistical data; * **Residential** buildings; **Tables** (Data); Fire detection **systems** ; Efficiency; Injuries
Identifiers: NTISFEMFDC
Section Headings: 89H (Building Industry Technology--Building Equipment, Furnishings, and Maintenance)

17/5/31 (Item 6 from file: 6)
DIALOG(R)File 6:NTIS

0995621 NTIS Accession Number: PB83-119040
Residential Detector Performance (Look at Deaths), 1979
Federal Emergency Management Agency, Washington, DC.
Corp. Source Codes: 057043000
28 Oct 80 277p
Languages: English
Journal Announcement: GRAI8304
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A13/MF A01
Country of Publication: United States
This document contains computer tables **generated** from data collected by the NFIRS for use as supportive data only and requires understanding and

familiarity of the data system.
Descriptors: Fires; *Statistical data; * **Residential** buildings; **Tables** (Data); Fire detection **systems** ; Efficiencies; Death; Mortality
Identifiers: NTISFEMFDC
Section Headings: 89H (Building Industry Technology--Building Equipment, Furnishings, and Maintenance)

17/5/32 (Item 7 from file: 6)
DIALOG(R)File 6:NTIS

0985112 NTIS Accession Number: PB82-258906/XAB
1979 Crosstab of Dollar Loss: Detector Recoded A
Federal Emergency Management Agency, Washington, DC.
Corp. Source Codes: 057043000
13 Dec 80 356p
Languages: English
Journal Announcement: GRAI8225
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A16/MF A01
Country of Publication: United States
This document contains computer tables **generated** from data collected by the NFIRS for use as supportive data only and requires understanding and familiarity of the data system.
Descriptors: Fires; *Fire detection **systems** ; *Statistical data; **Tables** (Data); Losses; **Residential** buildings
Identifiers: Mobile homes; NTISFEMFDC
Section Headings: 89H (Building Industry Technology--Building Equipment, Furnishings, and Maintenance)

17/5/33 (Item 8 from file: 6)
DIALOG(R)File 6:NTIS

0950091 NTIS Accession Number: PB82-175613/XAB
National Residential Passive Solar Energy Performance Tables
Oswald, R. ; Gruber, J.
Total Environmental Action, Inc., Harrisville, NH.
Corp. Source Codes: 066795000
Sponsor: Department of Housing and Urban Development, Washington, DC.
Report No.: HUD-0002239
Aug 81 446p
Languages: English
Journal Announcement: GRAI8212
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A19/MF A01
Country of Publication: United States
These National Residential Passive Solar Energy Performance Tables have been developed for HUD so that annual net energy savings from residential passive **systems** could be determined for any location within the country. The **tables** are applicable to **residential** buildings containing one to four dwelling units, for both newly constructed passive buildings and buildings where the passive systems have been retrofitted on to an existing structure. The energy savings represent average performance of various passive solar energy systems in typical residential buildings. The values are therefore not precise for a particular building and should not be used as a tool in evaluating a specific passive system design. Energy savings listed in the tables combine the annual heating energy savings as well as the incremental annual cooling load penalty caused by the passive solar energy systems. The procedures used for determining the energy savings are

described for both new residential construction and retrofit passive systems. The assumptions and methods used in constructing the tables are described, and examples of the procedures for various types of systems are given. Energy savings for retrofit passive systems are determined by either of two different procedures depending on whether or not the retrofit system adds to the heated living area of the building. Tables are given for each procedures: **Tables** for New **Residential** Construction and the **Tables** for Retrofit **Systems** . Diagrams and 14 references re provided. (**Author** abstract **modified**).

Descriptors: *Residential buildings; Performance evaluation; Tables(Data)

Identifiers: *Passive solar heating systems; Energy conservation; NTISHUDPDR

Section Headings: 97N (Energy--Solar Energy); 89B (Building Industry Technology--Architectural Design and Environmental Engineering)

17/5/34 (Item 9 from file: 6)

DIALOG(R)File 6:NTIS

0847842 NTIS Accession Number: ORNL-5552/XAB

Buildings Energy Use Data Book. Edition 2

Blue, J. L. ; Lowe, K. H. ; Hurlbut, B. J. ; Liepins, G. E. ; Rose, A. B.

Oak Ridge National Lab., TN.

Corp. Source Codes: 4832000

Sponsor: Department of Energy, Washington, DC.

Report No.: ORNL-5363(2ED.)

Dec 79 706p

Languages: English

Journal Announcement: GRAI8025; NSA0500

Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.

NTIS Prices: PC A99/MF A01

Country of Publication: United States

Contract No.: W-7405-ENG-26

This document is a statistical compendium designed for use as a desk-top reference. The data book represents an assembly and display of statistics that characterize current and past energy end-use activities in the residential and commercial sectors and presents data on other factors that influence energy use in these sectors. The purpose of the publication is to present a large amount of relevant data in an easily retrievable and usable format with the statistical data presented in the form of tables, graphs, and charts. The topics covered in the nine chapters include: (1) building stock characteristics, including construction trends, inventories, and physical and thermal characteristics; (2) appliance shipments, inventories, prices, and energy utilization efficiencies; (3) fuel production, consumption, and prices for the major energy sources (electricity, natural gas, liquid petroleum, and coal); (4) demographic and climatic variables, including data on energy use vs population by region and indicators of social **changes** that affect household energy consumption; (5) national economic determinants providing data on employment and unemployment, level of consumer spending, prices, government activity, and the effect of government monetary policy on the Gross National Product; (6) an overview of solar energy technology, governmental interactions, market activity, and future prospects; (7) community systems presenting data on **alternative** energy sources and technological options for conserving nonrenewable energy use in the major community subsystems - heating, cooling, hot water, electricity, and solid and liquid waste treatment; (8) school and hospital characteristics, inventory, and energy utilization; and (9) a review of selected analyses of energy use in the residential and commercial sectors. Data sources are listed at the end of each chapter. (ERA citation 05:024244)

Descriptors: Commercial buildings; *Energy consumption; *Hospitals; *Residential buildings; *School buildings; Appliances; Commercial sector; Construction; Data compilation; Forecasting; Graphs; Heating **systems** ; Lighting **systems** ; National energy act; Numerical data; Power demand;

Residential sector; Statistics; **Tables**
Identifiers: ERDA/320100; ERDA/298000; NTISDE
Section Headings: 97B (Energy--Energy Use, Supply, and Demand)

17/5/35 (Item 10 from file: 6)
DIALOG(R)File 6:NTIS

0821441 NTIS Accession Number: DOE/CS-0118/XAB
Proposed Energy-Performance Standards for New Buildings: Standard Building Operating Conditions. Technical Support Document
Department of Energy, Washington, DC.
Corp. Source Codes: 052661000; 9505475
Nov 79 79p
Languages: English
Journal Announcement: GRAI8016; NSA0500
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A05/MF A01
Country of Publication: United States
The process of developing Energy Budget Levels for new commercial buildings, in conjunction with the energy-performance standards for new buildings, includes the use of energy-analysis computer programs. These programs are used to estimate the design energy requirements of randomly selected commercial buildings comprising the study sample in both the Phase I and Phase 2 studies conducted by the American Institute of Architects Research Corporation. The input to these programs includes a set of data known as the Standard Building Operating Conditions (SBOC). These SBOC consist of temperatures, human-occupancy densities and profiles, lighting-usage profiles, and the like. They describe typical conditions under which a commercial or multifamily residential building would operate during the course of a day. This report (a) describes which building operating conditions were standardized, and how this was done in the AIA/RC team research efforts in Phases 1 and 2, which developed an information base for use by DOE in the development of the standards; (b) discusses **alternative** ways that SBOC may be applied in a regulatory compliance context, and the advantages and disadvantages of each **alternative** ; (c) examines some of the implications of the standardization of operating conditions; and (d) provides, for use with the Standard Evaluation Technique, SBOC that are reasonable, based on the research conducted, and that provides an equitable basis for comparing annual Design Energy Consumption estimates of buildings against Design Energy Budgets. (ERA citation 05:010241)
Descriptors: Buildings; Commercial buildings; Energy analysis; Energy consumption; Energy efficiency; Evaluated data; Lighting **systems** ; Operation; **Residential** buildings; Standards; **Tables** ; Temperature dependence
Identifiers: ERDA/320100; ERDA/298000; NTISDE
Section Headings: 97B (Energy--Energy Use, Supply, and Demand); 89B (Building Industry Technology--Architectural Design and Environmental Engineering)

17/5/36 (Item 11 from file: 6)
DIALOG(R)File 6:NTIS

0778210 NTIS Accession Number: PNL-2963/XAB
Preliminary Review of NECPA Generated **Information Requirements for the Office of Conservation and Solar Applications**
Rivera, R. G. ; Nieves, A. L.
Battelle Pacific Northwest Labs., Richland, WA.
Corp. Source Codes: 9500022
Sponsor: Department of Energy.
8 Mar 79 64p

Languages: English
Journal Announcement: GRAI7923; NSA0400
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A04/MF A01
Contract No.: EY-76-C-06-1830
Effective implementation of energy-conservation policy requires large quantities of various types of good-quality, timely data. To obtain the desired data, the information requirements must first be identified so that they can be communicated in a justifiable form to the Energy Information Administration (EIA) and other data-collecting organizations. This report represents the initial results of an effort to describe the general information needed by the Office of Conservation and Solar Applications (CS) to carry out their responsibility in implementing the National Energy Conservation Policy Act (NECPA). The assessment of the NECPA- **generated** information requirements is organized around the conservation programs for utilities, residences, industry, Federal and public buildings, and transportation. This assessment identifies the factors that **generate** the information requirements (sections, parts, and titles of NECPA), describes the general information needed to implement the act, and references potential sources of data. Appendix A contains a summary of this assessment in table form. (ERA citation 04:043213)
Descriptors: Energy conservation; *National Energy Act; Commercial sector ; Communications; Data; Data acquisition; Federal buildings; Implementation ; Industry; Information; Information needs; Public buildings; Public utilities; **Residential** sector; **Tables** ; Transportation **systems**
Identifiers: ERDA/291000; NTISDE
Section Headings: 97G (Energy--Policies, Regulations, and Studies)

17/5/37 (Item 12 from file: 6)
DIALOG(R)File 6:NTIS

0621693 NTIS Accession Number: HRP-0014058/2/XAB
Study of Georgia's Services for the Mentally Retarded. Volume I
Atlanta Association for Retarded Children, Inc., Ga.
Jan 72 122p
Journal Announcement: GRAI7712
Available from ERIC Document Reproduction Service, P.O. Box 190, Arlington, VA 22210 as ED 088 251.
NTIS Prices: Not available NTIS
Presented is the first of two volumes reporting on a 2-year study of Georgia's services to the mentally retarded by the Atlanta Association for Retarded Children (AARC). Discussed in the section on organization, philosophy and methodology is the concept of normalization as an underlying philosophy of AARC. Briefly described are model programs observed in Denmark, Sweden, Belgium, the Netherlands, England, Wisconsin, and Connecticut. A model comprehensive service system and existing community services are described in terms of the following areas: diagnosis and evaluation, family services, mental and physical health services, education and training services, work training, economic-legal supportive services, **recreation** services, religious training, transportation, and residential services. Noted is visitation of existing residential services by AARC staff members to determine current status of services. Detailed are evaluations of three special purpose residential facilities and three multipurpose residential facilities. Recommendations are given in the areas of: comprehensive mental retardation programs, specialized residential programs, improvement of existing residential facilities, and program planning. Examples of recommendations are funding priority for community based small group homes and admission to State institutions only for retardates whose needs cannot be met in the community. Among appendixes are the text of a Declaration of Rights, a listing of reference materials, the questionnaire used in the **residential** study, and a **chart** of the model comprehensive service **system** . (ERIC).
Descriptors: *Mental health care; *Georgia; Patients; Long term care;

Inpatients; Health care services; Ambulatory health care
Identifiers: *Mental deficiency; HRP/KF; HRP/KB; HRP/KAB; HRP/ZC; HRPGEO/YGA; HRPOCC/XZ; Mental health facilities; NTISHRANHP
Section Headings: 44K (Health Care--Health Services)

17/5/38 (Item 13 from file: 6)
DIALOG(R)File 6:NTIS

0219038 NTIS Accession Number: AD-702 592/XAB
An Interactive Graphical Display Monitor in a Batch Processing Environment with Remote Entry
Bond, A. H. ; Rightnour, J. ; Coles, L. S.
Carnegie-Mellon Univ Pittsburgh Pa Dept of Computer Science
Corp. Source Codes: 403081
Jun 69 11p
Document Type: Journal article
Journal Announcement: USGRDR7009
Revision of report dated Nov 68.
Pub. in Computer Systems, v12 n11 p595-604 Nov 69.
NTIS Prices: Not available NTIS
Contract No.: F44620-67-C-0058; AF-9749; 974901
A graphic monitor program is described. It was developed for the CDC G21 computer, which is a general purpose, batch-processing system with remote entry. The existing G21 **system** and the graphics hardware are described. The **graphic** monitor is a **resident** auxiliary monitor which provides comprehensive managerial capability over the graphical **system** in response to commands from the human user. It also will respond to commands from a user program through a similar interface, where routine calls take the place of manual actions. Thus the human and program can interact on a symmetrical and equal basis through the medium of the graphic monitor. The choices made in designing the graphic monitor, given the constraints of the existing hardware and computer system, are discussed. The structure of the monitor program and the human and program interfaces are described. There is also a transient swapping version with a small resident part, and provision for swapped used submonitors. (**Author**)
Descriptors: *Computers; *Programming(Computers); Graphics; Display systems; Man-machine systems; Interactions; Interfaces; Input-output devices; Data processing systems; Time sharing; Reprints
Identifiers: *Interactive ocmputer graphics; *Monitor routines; Batch processing; CDC G21 computers
Section Headings: 62A (Computers, Control, and Information Theory--Computer Hardware)

17/5/39 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

14296638 PASCAL No.: 99-0503258
A study on the development of transmission-type extrinsic Fabry-Perot interferometric optical fiber sensor
KIM S H; LEE J J; LEE D C; KWON I B
Department of Mechanical Engineering, Korea Advanced Institute of Science and Technology, Taejon 305-701, Korea, Republic of; Korea Research Institute of Standards and Science, Taejon 305-600, Korea, Republic of
Journal: Journal of lightwave technology, 1999, 17 (10) 1869-1874
ISSN: 0733-8724 CODEN: JLTEDG Availability: INIST-20142; 354000088204590190
No. of Refs.: 16 ref.
Document Type: P (Serial) ; A (Analytic)
Country of Publication: United States
Language: English
The conventional reflection-type extrinsic Fabry-Perot interferometric (EFPI) optical fiber sensor has good sensitivity and resolution compared with other types of optical fiber sensors. However, they have the disadvantage that the distinction of strain direction of EFPI is difficult

because of measurement method by only fringe counting. This paper presents the newly developed transmission-type EFPI (**TEFPI**) optical fiber sensor, which has been improved by additional functions, and whose measuring **system** differs from that of the reflection-type EFPI optical fiber sensors using a single-mode fiber (SMF) and multimode (MMF) fibers as light guides and reflectors, respectively. The output signal of the **TEFPI** optical fiber sensor was analyzed with the uniform plane wave-based model, the SMF power distribution-hased model and the splice loss-based model; the analyzed sign were then verified experimentally. Based on the results of analysis, the **TEFPI** optical fiber sensor was fabricated using two single-mode fibers connected to the light source and optical receiver; this was then used in strain measurement. The strain measured by the **TEFPI** optical fiber sensor was compared with that measured by the electric strain gauge.

English Descriptors: Optical fiber; Fabry Perot interferometer; Measuring **system** ; Single mode fiber; Light reflection; Signal analysis; Experimental result; Circuit design; Light source; Optical receiver; Multimode fiber; Optical fiber sensor

French Descriptors: Fibre optique; Interferometre Fabry Perot; **Systeme** mesure; Fibre monomode; Reflexion lumiere; Analyse signal; Resultat experimental; Conception circuit; Source lumineuse; Recepteur optique; Jauge contrainte; Fibre multimode; Capteur fibre optique

Classification Codes: 001D03G02C1

17/5/40 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

12625200 PASCAL No.: 96-0317916
Stochastic dislocation patterning during cyclic plastic deformation : A theory of the formation **of** persistent **slip band and** matrix **structures**
HAEHNER P
European Commission, Institute for Advanced Materials, TP 750, Joint Research Centre, 21020 Ispra, Italy
Journal: Applied physics. A, Materials science & processing, 1996, 63 (1) 45-55
Availability: INIST-16194A; 354000060049400070
No. of Refs.: 39 ref.
Document Type: P (Serial) ; A (Analytic)
Country of Publication: Germany
Language: English
A dislocation dynamical theory is developed for the formation of dipole dislocation patterns during cyclic plastic deformation in single glide. The stochastic dislocation dynamics adopted is suitable to account, in terms of a fluctuating effective medium, for the effects of long-range dislocation interactions on a mesoscopic scale. The theory can explain the occurrence of a matrix structure and persistent slip bands as a result of evolutionary processes, it gives the intrinsic strain amplitudes and the characteristic wavelength of these structures, and it allows for an interpretation of the structural **changes** associated with **changes** of the deformation conditions. Quantitative results are in good agreement with experimental observations.

English Descriptors: Theoretical study; Dynamic theory; Dislocation dipole; Dislocations; Plastic deformation; Slip; Stochastic processes

French Descriptors: Etude theorique; Theorie dynamique; Dipole dislocation; Dislocation; Deformation plastique; Glissement; Processus stochastique; 6172B; 6220F; 8140L

Classification Codes: 001B60A72B; 001B60B20F; 001B80A40L

17/5/41 (Item 3 from file: 144)
DIALOG(R)File 144:Pascal

10875229 PASCAL No.: 93-0384593
Theoretical characteristics of a tunable two-electrode Fabry-Perot (TEFP) laser diode
LE BIHAN J; GOUJON J M; AUFFRET R; MOUHAMAD JAMIL CHAWKI
ENIB, lab. RESO, 29608 Brest, France; CNET, LAB/SMR/ESO, 22301 Lannion, France
Journal: Journal of lightwave technology, 1992, 10 (12) 1931-1934
ISSN: 0733-8724 CODEN: JLTEDG Availability: INIST-20142; 354000032910110220
No. of Refs.: 10 ref.
Document Type: P (Serial) ; A (Analytic)
Country of Publication: USA
Language: English
Tuning analysis of a two-electrode Fabry-Perot laser diode has been studied theoretically. Theoretical power and wavelength characteristics have been derived from an analytical model. This two-electrode Fabry-Perot laser presents a wide tuning range, which makes it able to operate in FM and AM optical communication **systems**

English Descriptors: Injection laser; Performance characteristic; Calculating method; Theoretical study
French Descriptors: Laser injection; Caracteristique fonctionnement; Methode calcul; Etude theorique

Classification Codes: 001D03F15

17/5/42 (Item 4 from file: 144)
DIALOG(R)File 144:Pascal

04847904 PASCAL No.: 83-0093728
lang. rus
(Generation et utilisation des tables **non** residentielles **dans le** systeme **du concentrateur de terminaux)**
MIKUSHAUSKAS R
Journal: Programmirovanie E.V.M., 1981 (5) 125-136
ISSN: 508101 Availability: CNRS-16116G
No. of Refs.: 4 ref.
Document Type: P (Serial) ; A (Analytic)
Country of Publication: Union of Soviet Socialist Republics
Language: Russian Summary Language: Lithuanian; English
Definition, structure et fonction des tables non residentielles avec leurs programmes **generateurs** . Description de l'algorithme d'utilisation des tables non residentielles dans le logiciel d'un concentrateur de terminaux

English Descriptors: Computer system; Operating system; Remote concentrator ; Terminal; System configuration; Software

French Descriptors: Systeme informatique; Systeme exploitation; Concentrateur ligne; Terminal; Organisation systeme; Logiciel

Classification Codes: 110C03D02

17/5/43 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

04978785 Genuine Article#: UW816 Number of References: 41

Title: STOCHASTIC DISLOCATION PATTERNING DURING CYCLIC PLASTIC-DEFORMATION - A THEORY OF THE FORMATION OF PERSISTENT SLIP BAND AND MATRIX STRUCTURES

Author(s): HAHNER P
Corporate Source: COMMISS EUROPEAN COMMUNITIES,INST ADV MAT,JOINTRES CTR,TP 750/I-21020 ISPRA//ITALY/

Journal: APPLIED PHYSICS A-MATERIALS SCIENCE & PROCESSING, 1996, V63, N1 (JUL), P45-55
ISSN: 0721-7250
Language: ENGLISH Document Type: ARTICLE
Geographic Location: ITALY
Subfile: SciSearch; CC PHYS--Current Contents, Physical, Chemical & Earth Sciences
Journal Subject Category: PHYSICS, APPLIED

Abstract: A dislocation dynamical theory is developed for the formation of dipole dislocation patterns during cyclic plastic deformation in single glide. The stochastic dislocation dynamics adopted is suitable to account, in terms of a fluctuating effective medium, for the effects of long-range dislocation interactions on a mesoscopic scale. The theory can explain the occurrence of a matrix structure and persistent slip bands as a result of evolutionary processes, it gives the intrinsic strain amplitudes and the characteristic wavelength of these structures, and it allows for an interpretation of the structural **changes** associated with **changes** of the deformation conditions. Quantitative results are in good agreement with experimental observations.

Identifiers--KeyWords Plus: COPPER SINGLE-CRYSTALS; DIMENSIONAL CONSIDERATIONS; FATIGUE; STABILITY; MODEL; FCC; BEHAVIOR; METALS
Research Fronts: 94-5272 006 (CYCLIC STRESS-STRAIN RESPONSE; POLYCRYSTALLINE COPPER; DISLOCATION-STRUCTURES OF AISI 316L STAINLESS-STEEL; PERSISTENT SLIP BANDS; FATIGUE DAMAGE)

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ESSMANN U, 1988, P433, BASIC MECH FATIGUE
ESSMANN U, IN PRESS MAT SCI E A
ESSMANN U, 1979, V40, P731, PHIL MAG A
FRANEK A, 1991, V64, P497, PHILOS MAG A
HAHNER P, 1996, V62, P473, APPL PHYS A
HAHNER P, 1996, P514, P 8 INT S CONT MOD D
HAHNER P, 1996, V34, P435, SCRIPTA MATER
HAHNER P, UNPUB ACTA METALL MA
HANCOCK JR, 1969, V17, P77, ACTA METALL
HOLZWARTH U, 1994, V58, P197, APPL PHYS A-MATER
HOLZWARTH U, 1993, V57, P131, APPL PHYS A-SOLID
HOLZWARTH U, 1993, V164, P206, MAT SCI ENG A-STRUCT
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MUGHRABI H, 1978, V33, P207, MATER SCI ENG
MUGHRABI H, 1987, V104, P107, PHYS STATUS SOLIDI A
MUGHRABI H, 1985, V323, P244, PUBL I METALS
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PEDERSEN OB, 1981, V29, P1843, ACTA METALL
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WALGRAEF D, 1985, V23, P1359, INT J ENG SCI
WALGRAEF D, 1985, V23, P1365, INT J ENG SCI
WILKENS M, 1969, V17, P1155, ACTA METALL
WILKENS M, 1980, V71, P376, Z METALLKD
WINTER AT, 1974, V30, P719, PHILOS MAG

17/5/44 (Item 2 from file: 34)

03584254 Genuine Article#: PP053 Number of References: 2
Title: MECHANICAL VAPOR COMPRESSION TO TREAT OIL-FIELD PRODUCED WATER
Author(s): KOREN A; NADAV N
Corporate Source: IDE TECHNOL LTD,POB 591/RAANANA//ISRAEL/
Journal: DESALINATION, 1994, V98, N1-3 (SEP), P41-48
ISSN: 0011-9164
Language: ENGLISH Document Type: ARTICLE
Geographic Location: ISRAEL
Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences
Journal Subject Category: WATER RESOURCES; ENGINEERING, CHEMICAL
Abstract: Over the past 15 years steam injection has been the only method capable of significantly enhancing oil recovery in the German and Dutch oil fields producing a highly viscous crude. However, the steam injection has a negative impact on the oil reservoir pressure, since the steam to oil ratio is about 4. This means that for each produced barrel of oil, there is an accumulation of 4 barrels of condensed water coming from the injected steam.

The outcoming oil and water mixture is separated in decantation tanks. The oil is further processed and the remaining brine is a disposal stream.

The conventional method to dispose of the produced water is to pump it to separate reservoirs, such as a depleted underground gas reservoir, but this is **limited** to the **available** disposal capacity. Any other means to dispose the produced water to lakes or to rivers is prohibited by environmental regulations. The re-injection of the water back to the depleted reservoir is prohibited too based on the following:

Contamination of the potable quality ground water with oil through cracks in the **formation** because of the increased pressure of the reinjected water.

Raising the water **table** in adjacent **residential** areas due to the pressure of reinjected water, leading to the closing of ground water wells due to contamination.

Irreversible changes in underground locked crude pockets which may damage future oil exploration.

Based on careful investigations prepared by the oil companies operating in the German/Dutch oil fields it was decided to install a mechanical vapour compression unit to desalinate the produced water and use the distillate for boiler feed water, thus recycling the produced water and eliminating the previously mentioned drawbacks.

This paper outlines the process which allows the production of high quality boiler feed water for steam generation from produced water, eliminating the ecological dangers mentioned above, This is achieved by ensuring a permanent water balance in the oil reservoir in the form of a closed water cycle, thus preventing the excessive volume of injected steam and creating the continuous addition of water to the **system** either from the fresh water wells or other available water resources.
Cited References:
1ST MVC EVAPORATOR C, 1991

HINNERS GA, 1992, 4TH S BERL

17/5/45 (Item 3 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

02307051 Genuine Article#: KR949 Number of References: 10
Title: THEORETICAL CHARACTERISTICS OF A TUNABLE 2-ELECTRODE FABRY-PEROT (TEFP) LASER DIODE
Author(s): LEBIHAN J; GOUJON JM; AUFFRET R; CHAWKI MJ
Corporate Source: ECOLE NATL INGN BREST,LAB RESO,TECHNOPOLE BRESTIROISE,CP 15/F-29608 BREST//FRANCE/; CNET,LAB SMR ESO/F-22301 LANNION//FRANCE/
Journal: JOURNAL OF LIGHTWAVE TECHNOLOGY, 1992, V10, N12 (DEC), P1931-1934
ISSN: 0733-8724
Language: ENGLISH Document Type: ARTICLE
Geographic Location: FRANCE
Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences
Journal Subject Category: OPTICS
Abstract: Tuning analysis of a two-electrode Fabry-Perot laser diode has been studied theoretically. Theoretical power and wavelength characteristics have been derived from an analytical model. This two-electrode Fabry-Perot laser presents a wide tuning range, which makes it able to operate in FM and AM optical communication **systems** .
Research Fronts: 91-0227 002 (DFB LASERS; LINEWIDTH ENHANCEMENT FACTOR; DISTRIBUTED FEEDBACK; GAIN SATURATION CHARACTERISTICS; OPTICAL PULSES)
Cited References:
ADAMS MJ, 1985, V132, P58, IEE PROC-J
ADAMS MJ, 1985, V21, P609, IEEE J QUANTUM ELECT
ADAMS MJ, 1989, V21, P15, OPT QUANT ELECTRON
CHAWKI MJ, 1991, V27, P417, ELECTRON LETT
CHAWKI MJ, 1990, V11, P63, J OPT COMMUN
KOTAKI Y, 1988, V24, P503, ELECTRON LETT
MARCUSE D, 1983, V19, P63, IEEE J QUANTUM ELECT
MCDONALD D, 1991, 3RD BANG S COMM
ODOWD RF, 1988, V20, P383, OPT QUANT ELECTRON
RIGOLLE PJ, 1991, V12, P69, J OPT COMMUN

17/5/46 (Item 4 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

02043399 Genuine Article#: JX039 Number of References: 0
Title: PICTURE CONVERSION FOR HIGH-DEFINITION GRAPHICS
Author(s): PANK RA
Corporate Source: QUANTEL LTD/NEWBURY RG13 2NE/BERKS/ENGLAND/
Journal: SMPTE JOURNAL-SOCIETY OF MOTION PICTURE AND TELEVISION ENGINEERS, 1992, V101, N11 (NOV), P797-799
ISSN: 0036-1682
Language: ENGLISH Document Type: ARTICLE
Geographic Location: ENGLAND
Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences
Journal Subject Category: INSTRUMENTS & INSTRUMENTATION; TELECOMMUNICATIONS ; PHOTOGRAPHIC TECHNOLOGY
Abstract: In the high-definition (HD) production environment the use of 1125/60 and 1250/50 formats **creates** the need for conversion at the HD level, while down and upconversions to the established 525/60 and 625/50 broadcast systems are also required. In the particular case of stills used in **graphics systems** , their existing **resident** facilities can be employed to provide high-quality conversions automatically. In this way images may be passed between systems for use in the different HD and broadcast standards. In addition, graphic elements may be successfully sourced from any format to make a composite image. Such techniques have an obvious long-term application as well as helping users to negotiate the current HD standards

"minefield."

17/5/47 (Item 1 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00807238 E94071558208
An expert system for integrated protection design with configurable distribution circuits: Part I
(Netzschutzentwurf mit integriertem Expertensystem und Verteilungsnetz-Darstellungen: Teil 1)
Broadwater, RP; Thompson, JC; Rahman, S; Sargent, A
Virginia Polytech. Inst. a. State Univ., Blacksburg, USA; Arkansas Power a. Light, Hot Springs, USA
IEEE Transactions on Power Delivery, v9, n2, pp1115-1121, 1994
Document type: journal article Language: English
Record type: Abstract
ISSN: 0885-8977

ABSTRACT:
An integrated expert system for protection system design has been developed, for an engineering workstation, using a relational database management system. The expert system incorporated both procedural and declarative, or query operating modes. Rules dealing with the coordination, placement and selection of protection devices are used to incorporate expert knowledge into the knowledge base. The protection system designer controls which rules are implemented in the design. The expert system incorporates the key elements and requirements data integration, relational database management system and graphical user interface. Data integration is achieved by way of the relational database **system** and by the use of **in - memory** objects. A **graphical** user interface is provided for the designer. The expert **system** provides user **modifiable** rules that reflect designer knowledge and control decision processing. Configurable circuits are checked for coordination of tie-line devices. Additional conclusions will be presented in part 2.

DESCRIPTORS: POWER SYSTEM PROTECTION; SYSTEMS DESIGN; COMPUTER AIDED DESIGN ; EXPERT SYSTEMS; SYSTEMS INTEGRATION; DATABASE MANAGEMENT SYSTEM; RELATIONAL DATABASES; DISTRIBUTION NETWORKS; COMPOSITE POWER SYSTEM; SYSTEM SIMULATION; USER INTERFACES; BEHAVIOUR--PERFORMANCE; SYSTEM DESCRIPTION; DECISION MAKING
IDENTIFIERS: Netzschutzentwurf; Expertensystem; CAD

17/5/48 (Item 2 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00599450 I92071539927
The implementation of FDL, a functional database language
(Implementierung der funktionalen Datenbanksprache FDL)
Poulovassilis, A
King's Coll. London, UK
Computer Journal, London, v35, n2, pp119-128, 1992
Document type: journal article Language: English
Record type: Abstract
ISSN: 0010-4620

ABSTRACT:
The implementation of the functional database language FDL is described. FDL improves upon previous languages with a functional data model by allowing any computable function to be defined and stored and by supporting arbitrarily nested data types which are all persistent. All functions are updated incrementally by the insertion and deletion of equations, and an integrity sub-system verifies updates against the declared semantic integrity constraints. The **author** shows how a binary relational storage structure is used to support all of FDL's persistent data. He also shows

how the technique of graph reduction from functional programming languages is **modified** for the evaluation of FDL queries. Finally, he compares the implementation with that of related languages.

DESCRIPTORS: DATA MODELS; DATABASE MANAGEMENT SYSTEM; FUNCTIONAL PROGRAMMING; QUERY LANGUAGES; MEMORY MANAGEMENT; DATA BANK; DATA FORMAT; PROGRAMMING LANGUAGES; DATA INTEGRITY
IDENTIFIERS: FUNCTIONAL DATABASE LANGUAGE FDL; FUNCTIONAL DATA MODEL; COMPUTABLE FUNCTION; ARBITRARILY NESTED DATA TYPES; INTEGRITY SUB **SYSTEM** ; DECLARED SEMANTIC INTEGRITY CONSTRAINTS; BINARY RELATIONAL STORAGE STRUCTURE; **PERSISTENT** DATA; **GRAPH** REDUCTION; FUNCTIONAL PROGRAMMING **LANGUAGES** ; FDL QUERIES; Datenbank; funktionale Programmierung

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Set     Items   Descript
S1         14   TEFP? OR TEFPFEC OR EXTEND?()FAST()PATH?
S2      72109   PERSISTENT? OR RESIDENT? OR "IN"()(MEMOR? OR SRAM OR RAM) -
             OR TSR
S3       3616   S2(3N)(TABLE? OR GRAPH? OR CHART? OR TUPL? OR MATRIX? OR M-
             ATRICE?)
S4    1150130   SYNTAX? OR FORMAT? OR LANGUAGE? OR SCHEMA? OR SYSTEM?
S5      44132   (ACCESS? OR AVAILAB?)(4N)(LIMIT? OR PARAMET? OR OPEN OR CL-
             OSED OR PARTIAL? OR TIER? OR HIERARCH?)
S6       3533   S3 AND S4
S7       6438   (DROP? OR END? OR KILL? OR STOP?)(3N)(COMMAND? OR SHUTDOWN?
              OR POWERDOWN OR (POWER OR SHUT)()(DOWN OR OFF))
S8         28   S3(S)S4(S)S5
S9          5   S1 AND S2
S10        20   S3(S)S7
S11        49   S8 OR S9 OR S10
S12        23   S11 AND IC=G06F?
S13        23   IDPAT (sorted in duplicate/non-duplicate order)
S14        23   IDPAT (primary/non-duplicate records only)
S15    954532   CREAT? OR EDIT? OR MODIF? OR GENERAT? OR RECREAT? OR REDO -
             OR REGENERAT? OR GENERAT?
S16        40   S3(5N)S4(5N)S15
S17         4   S16 AND IC=(G06F-017? OR G06F-007?)
S18         4   IDPAT (sorted in duplicate/non-duplicate order)
S19         4   IDPAT (primary/non-duplicate records only)
File 348:EUROPEAN PATENTS 1978-2002/Sep W03
         (c) 2002 European Patent Office
File 349:PCT FULLTEXT 1983-2002/UB=20020912,UT=20020905
         (c) 2002 WIPO/Univentio
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19/5/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01239309
METHOD FOR COMBINING TABLE DATA
VERFAHREN ZUM KOMBINIEREN VON TABELLEN-DATEN
PROCEDE DE COMBINAISON DE DONNEES DE TABLEAU
PATENT ASSIGNEE:
Turbo Data Laboratory Inc., (3191480), Court house Kikuna 804, 1101-7, Matsumi-cho 4-chome, Kanagawa-ku, Yokomaha-shi, Kanagawa 221-0005, (JP), (Applicant designated States: all)
INVENTOR:
FURUSHO, Shinji, Court house Kikuna 804, 1101-7, Matsumi-cho 4-chome, Kanagawa-ku, Yokohama-shi, Kanagawa 221-0005, (JP)
LEGAL REPRESENTATIVE:
Zimmermann, Gerd Heinrich (78963), Zimmermann & Partner, P.O. Box 33 09 20, 80069 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 1191462 A1 020327 (Basic)
WO 200073939 001207
APPLICATION (CC, No, Date): EP 2000929916 000530; WO 2000JP3465 000530
PRIORITY (CC, No, Date): JP 99151156 990531
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **G06F-017/30** ; G06F-019/00
CITED REFERENCES (WO A):
JP 63298626 A
UKI: 'SybaseIQ: Dokuji data kouzou ni yoru data warehouse eno approach' TECHNICAL RESEARCH REPORT, THE INSTITUTE OF ELECTRONICS, INFORMATION AND COMMUNICATION ENGINEERS (AI97-42) vol. 97, no. 415, 02 December 1997, pages 51 - 56
TORII ET AL.: 'Relational database no shori sokudo koujou wo hakaru CPU naizougata databease processor merge enzan no pipeline jikkou ni yori sort shori wo kousokuka' NIKKEI ELECTRONICS vol. 414, 09 February 1987, pages 185 - 206;

ABSTRACT EP 1191462 A1
The present invention provides a structure for table-format data with a small data size whereby a plurality of tables of table-format data can be joined as desired, a method of concatenating table-format data, and a method for displaying concatenated table-format data.
In this method, each table of table-format data is constructed in a manner such that each table is divided into one or more information blocks consisting of: a value list in which the field values are stored in the order of a field value number corresponding to the field value belonging to a specified field, and a pointer array in which pointer values for pointing to said field value numbers are stored in a unique record order. The concatenation of a plurality of tables of table-format data is performed by finding equivalent fields among a plurality of tables of table-format data, identifying the information blocks for said equivalent fields, and, in each of said plurality of tables of table-format data, comparing the value lists contained in said identified information blocks, and setting both value lists to the same values. At the time of setting said value lists to the same values, pointer values are added to associated pointer arrays in the information block to which that field value is added, and by making the value lists contained in the information blocks for specific fields in said plurality of tables of table-format data equivalent, concatenating the table-format data.
ABSTRACT WORD COUNT: 239
NOTE:
Figure number on first page: 11

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 010131 A1 International application. (Art. 158(1))
Application: 010131 A1 International application entering European phase

Application: 020327 [redacted] Published application with se[redacted]h report
Examination: 020327 A1 Date of request for examination: 20011130
LANGUAGE (Publication,Procedural,Application): English; English; Japanese
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200213	6945
SPEC A	(English)	200213	18326
Total word count - document A			25271
Total word count - document B			0
Total word count - documents A + B			25271

19/5/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00867528
Parallel searching technique
Verfahren zum Parallelrecherchieren
Technique de recherches paralleles
PATENT ASSIGNEE:
INTERNATIONAL COMPUTERS LIMITED, (233330), ICL House, Putney, London, SW15 1SW, (GB), (applicant designated states: DE;FR;GB)
INVENTOR:
Brown, Anthony Peter Graham, Hartford House, Vicarage Lane, Yateley, Camberley, Surrey GU17 7QR, (GB)
LEGAL REPRESENTATIVE:
Guyatt, Derek Charles et al (31325), Fujitsu Services Limited Observatory House Windsor Road, Slough Berkshire SL1 2EY, (GB)
PATENT (CC, No, Kind, Date): EP 795834 A1 970917 (Basic)
APPLICATION (CC, No, Date): EP 97300409 970122;
PRIORITY (CC, No, Date): GB 9605473 960315
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: **G06F-017/30**

ABSTRACT EP 795834 A1
A parallel query manager accepts a list of file extents to be searched and produces a number of search lists, one for each disk to be searched. The query manager first uses a mapper to find out how the database spaces are stored on disk. It then matches the search extent list with the mapping information to determine which parts of which disks are to be searched. It then initiates several searches in parallel so that all the affected disks can be kept busy at the same time. The query manager then checks for return data on each stream, and merges the results.
ABSTRACT WORD COUNT: 104

LEGAL STATUS (Type, Pub Date, Kind, Text):

Change:	020515	A1	Legal representative(s) changed 20020325
Application:	970917	A1	Published application (A1with Search Report ;A2without Search Report)
Assignee:	020731	A1	Transfer of rights to new applicant: Fujitsu Services Limited (233335) 26 Finsbury Square London, EC2A 1SL GB
Examination:	980325	A1	Date of filing of request for examination: 980123

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9709W2	431
SPEC A	(English)	9709W2	2545
Total word count - document A			2976
Total word count - document B			0
Total word count - documents A + B			2976

19/5/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00798908

Method for querying incrementally maintained transactional databases
Suchverfahren fur standig unterhaltene Transaktionsdatenbanken
Procede de recherche pour des bases de donnees transactionelles maintenues en continu

PATENT ASSIGNEE:
AT&T IPM Corp., (1907680), 2333 Ponce de Leon Boulevard, Coral Gables, Florida 33134, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Jagadish, Hosagrahar Visvesvaraya, 16 Beech Avenue, Berkeley Heights, Union, New Jersey 07922, (US)
Silberschatz, Abraham, 19A Hillside Avenue, Summit, New Jersey 07901, (US)
Mumick, Inderpal Singh, 85 Swanson Circle, Berkeley Heights, Union, New Jersey 07922, (US)
LEGAL REPRESENTATIVE:
Buckley, Christopher Simon Thirsk et al (28912), Lucent Technologies, 5 Mornington Road, Woodford Green, Essex IG8 0TU, (GB)
PATENT (CC, No, Kind, Date): EP 743609 A2 961120 (Basic)
APPLICATION (CC, No, Date): EP 96303413 960514;
PRIORITY (CC, No, Date): US 446170 950519
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: **G06F-017/30**

ABSTRACT EP 743609 A2

The chronicle data model of the present invention permits the capture, within the data model, of many computations common to transactional recording systems. An important aspect of the chronicle data model is incremental maintenance of materialized view in time independent of the size of the recorded stream.

The chronicle data model differs from the relational model in that it encapsulates within itself (1) support for aggregate, or summary, queries over sequences that may not be stored in their entirety, through the use of materialized (or persistent) views; and, (2) automatic incremental maintenance of persistent views as records are inserted into the sequence.

A chronicle data model can be implemented on top of a relational system. An aspect of this invention is to reduce the complexity of the application domains that need a chronicle system by encapsulating this model within the database. Within the chronicle data model of the present invention is disclosed: the type of summary queries that can be answered by using persistent views is determined, the complexity of incrementally maintaining the persistent views and development of a language ensuring low maintenance complexity independent of the sequence sizes. (see image in original document)
ABSTRACT WORD COUNT: 219

LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 961120 A2 Published application (A1with Search Report ;A2without Search Report)
Withdrawal: 970423 A2 Date on which the European patent application was withdrawn: 970227
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	1248
SPEC A	(English)	EPAB96	4991
Total word count - document A			6239
Total word count - document B			0
Total word count - documents A + B			6239

19/5/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00258295

Matrix concatenation in a graphics display system.
Aneinanderreihung von Matrizen in einem Grafiksichtsystem.
Concatenation de matrices dans un systeme d'affichage graphique.

PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
Fiore, Anthony Michael, 189 North Manor Avenue, Kingston New York 12401, (US)
Hempel, Bruce Carlton, Box191 R.D. 1, Tivoli New York 12583, (US)
Laib, Gregory Donald, Route 1 Box 256C, West Hurley New York 12491, (US)
Liang, Bob Chao-Chu, Box 522 Ryan Drive, West Hurley New York 12491, (US)
LEGAL REPRESENTATIVE:
Burt, Roger James, Dr. (52152), IBM United Kingdom Limited Intellectual Property Department Hursley Park, Winchester Hampshire SO21 2JN, (GB)
PATENT (CC, No, Kind, Date): EP 261390 A2 880330 (Basic)
EP 261390 A3 910515
EP 261390 B1 931124
APPLICATION (CC, No, Date): EP 87111955 870818;
PRIORITY (CC, No, Date): US 912724 860926
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: **G06F-007/548** ; G06F-015/347; G06F-015/62
CITED REFERENCES (EP A):
IBM TECHNICAL DISCLOSURE BULLETIN, vol. 27, no. 1A, June 1984, pages 139-142, New York, US; A. KAFFASHAN et al.: "Coordinate transformation in a graphics display processor";

ABSTRACT EP 261390 A2

To avoid the overflow problem, in a graphics display system which employs matrix concatenation for coordinate transformation and matrix element precision equal to that inherent to the system, which can cause an out-of-bounds location of a data element, number translation shift factors are introduced for the last row of the matrix which when used to operate on matrix elements. This will maintain the elements within the physical boundaries of the graphics base by preventing overflow. The disclosed modification can be implemented in microcode in a commercially availably graphics display system such as the IBM 5080 Graphics System.

ABSTRACT WORD COUNT: 101

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	880330	A2	Published application (A1with Search Report ;A2without Search Report)
Examination:	880921	A2	Date of filing of request for examination: 880729
Search Report:	910515	A3	Separate publication of the European or International search report
Change:	910612	A2	Representative (change)
Change:	910703	A2	Obligatory supplementary classification (change)
Examination:	920610	A2	Date of despatch of first examination report: 920429
Change:	920930	A2	Representative (change)
Grant:	931124	B1	Granted patent
Oppn None:	941117	B1	No opposition filed
Lapse:	991020	B1	Date of lapse of European Patent in a contracting state (Country, date): IT 19931124,

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	603
CLAIMS B	(German)	EPBBF1	546
CLAIMS B	(French)	EPBBF1	698
SPEC B	(English)	EPBBF1	3463
Total word count - document A			0
Total word count - document B			5310
Total word count - documents A + B			5310

14/5/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00983606
Pipeline decoding system
Pipeline-System zur Dekodierung
Systeme pipeline de decodage
PATENT ASSIGNEE:
Discovision Associates, (260275), 2355 Main Street, Suite 200, Irvine, CA 92614, (US), (applicant designated states: AT;BE;CH;DE;FR;GB;IE;IT;LI;NL)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol BS6 1NA, (GB)
Sotheran, Martin William, The Ridings, Wick Lane, Stinchcombe, Dursley, Gloucestershire GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, CAM, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-Under-Edge, Gloucestershire GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 891089 A1 990113 (Basic)
APPLICATION (CC, No, Date): EP 98202149 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 674443 (EP 953013018)
INTERNATIONAL PATENT CLASS: H04N-007/24; **G06F-019/00** ; **G06F-013/00** ; **G06F-009/38**

ABSTRACT EP 891089 A1
A pipeline processing machine having a plurality of reconfigurable processing stages interconnected by a two-wire interface bus, one of said processing stages being a spatial decoder; a second of said stages being a token generator for generating control tokens and data tokens for passage along said two-wire interface; said machine comprising :
a token decode means positioned in said spatial decoder for recognizing certain of said tokens as control tokens pertinent to said spatial decoder and for configuring said spatial decoder for spatially decoding said data tokens following said control token into a first decoded format ; and
a further one of said stages being a temporal decoder positioned downstream in said pipeline from said spatial decoder; a second token decode means positioned in said temporal decoder for recognizing certain of said tokens as control tokens pertinent to said temporal decoder and for configuring said temporal decoder for temporally decoding said data tokens following said control token into a second decoded format.
ABSTRACT WORD COUNT: 165

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	990113 A1	Published application (A1with Search Report ;A2without Search Report)
Examination:	990113 A1	Date of filing of request for examination: 980626
Examination:	990901 A1	Date of dispatch of the first examination report: 19990713

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9902	165
SPEC A	(English)	9902	127403
Total word count - document A			127568
Total word count - document B			0

Total word count - docum[redacted]s A + B 127568

14/5/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00975324
Pipeline decoding system
Pipeline-System zur Dekodierung
Systeme pipeline de decodage
PATENT ASSIGNEE:
Discovision Associates, (260275), 2355 Main Street, Suite 200, Irvine, CA 92614, (US), (Proprietor designated states: all)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol BS16 1NA, (GB)
Sotheran, Martin William, The Ridings, Wick Lane, Stinchcombe, Dursley, Gloucestershire GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-Under-Edge, Gloucesterhire GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 884910 A1 981216 (Basic)
EP 884910 B1 010509
APPLICATION (CC, No, Date): EP 98202132 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 674443 (EP 95301301)
INTERNATIONAL PATENT CLASS: H04N-007/24; **G06F-013/00** ; **G06F-009/38**
CITED PATENTS (EP B): EP 572766 A; EP 576749 A; WO 94/25935 A
CITED REFERENCES (EP B):
MAYER A C: "THE ARCHITECTURE OF A SINGLE-CHIP PROCESSOR ARRAY FOR VIDEOCOMPRESSION" PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON CONSUMER ELECTRONICS, ROSEMONT, JUNE 8 - 10, 1993, no. CONF. 12, 8 June 1993, page 294/295 XP000427624 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS
KAORU UCHIDA ET AL: "A PIPELINED DATAFLOW DATAFLOW PROCESSOR ARCHITECTURE BASED ON A VARIABLE LENGTH TOKEN CONCEPT" ARCHITECTURE, UNIVERSITY PARK, AUG. 15 - 19, 1988, vol. 1, no. CONF. 17, 15 August 1988, pages 209-216, XP000079309
YONG M CHONG: "A DATA-FLOW ARCHITECTURE FOR DIGITAL IMAGE PROCESSING" WESCON CONFERENCE RECORD,1 January 1984, pages 4/6 1-4/6 10, XP000565437
KOMORI S ET AL: "AN ELASTIC PIPELINE MECHANISM BY SELF-TIMED CIRCUITS" IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 23, no. 1, February 1988, pages 111-117, XP000051576;

ABSTRACT EP 884910 A1
A pipeline system having an inverse modeller stage and an inverse discrete cosine transform stage, comprising a processing stage, positioned between said inverse modeller stage and said inverse discrete cosine transform stage, responsive to tokens for processing data, wherein said tokens each comprise a plurality of data words, each said word including an extension indicator which indicates a presence or an absence of additional words in said token, a length of said token being determined by said extension indicators, whereby the length of said token can be unlimited;

wherein said tokens are communicated from said inverse modeller stage to said processing stage.
ABSTRACT WORD COUNT: 104
NOTE:

Figure number on first page: 76

LEGAL STATUS (Type, Pub Date, Kind, Text):

Change:	000607	A1	International Patent Classification changed: 20000419
Application:	981216	A1	Published application (A1with Search Report ;A2without Search Report)
Oppn None:	020502	B1	No opposition filed: 20020212
Lapse:	020403	B1	Date of lapse of European Patent in a contracting state (Country, date): AT 20010509, BE 20010509,
Grant:	010509	B1	Granted patent
Change:	000607	A1	Title of invention (French) changed: 20000419
Change:	000607	A1	Title of invention (English) changed: 20000419
Change:	000607	A1	Title of invention (German) changed: 20000419
Change:	000712	A1	International Patent Classification changed: 20000524
Change:	000712	A1	Title of invention (German) changed: 20000524
Change:	000712	A1	Title of invention (English) changed: 20000524
Change:	000712	A1	Title of invention (French) changed: 20000524
Lapse:	020320	B1	Date of lapse of European Patent in a contracting state (Country, date): BE 20010509,
Lapse:	020410	B1	Date of lapse of European Patent in a contracting state (Country, date): AT 20010509, BE 20010509, CH 20010509, LI 20010509,
Examination:	981216	A1	Date of filing of request for examination: 980626
Examination:	990901	A1	Date of dispatch of the first examination report: 19990713

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199851	498
CLAIMS B	(English)	200119	330
CLAIMS B	(German)	200119	308
CLAIMS B	(French)	200119	382
SPEC A	(English)	199851	126705
SPEC B	(English)	200119	122739
Total word count - document A			127222
Total word count - document B			123759
Total word count - documents A + B			250981

14/5/3 (Item 3 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00891605

Debugging apparatus for debugging a program
Vorrichtung zur Programmfehlerbeseitigung
Systeme de debogage d'un programme

PATENT ASSIGNEE:
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD., (216885), 1006, Oaza Kadoma, Kadoma-shi, Osaka 571-0050, (JP), (Proprietor designated states: all)

INVENTOR:
Nishibata Motohide, 4-9 Nakamachi, Kadoma-shi, Osaka-fu 571, (JP)
Iwamura, Yoshiyuki, 1-39-18, Kitayama, Hirakata-shi, Osaka-fu 573 01, (JP)
Sumi, Fumio, 5-8-404 Myoukenzaka, Katano-shi, Osaka-fu 571, (JP)

LEGAL REPRESENTATIVE:
Crawford, Andrew Birkby et al (29761), A.A. Thornton & Co. 235 High Holborn, London WC1V 7LE, (GB)

PATENT (CC, No, Kind, Date): EP 814404 A1 971229 (Basic)
EP 814404 B1 010131

APPLICATION (CC, No, Date): EP 97304271 970618;

PRIORITY (CC, No, Date): JP 96157841 960619

DESIGNATED STATES: DE; FR; GB; NL
INTERNATIONAL PATENT CLASS: **G06F-011/00**
CITED PATENTS (EP B): EP 588473 A; WO 92/15962 A; WO 95/29442 A
CITED REFERENCES (EP B):
ROBERT D. GRONLUND ET AL.: "The HP 64700 Embedded Debug Environment: A New Paradigm for Embedded System Integration and Debugging" HEWLETT-PACKARD JOURNAL., vol. 44, no. 2, April 1993, PALO ALTO US, pages 90-106, XP000360990;

ABSTRACT EP 814404 A1
A debugging apparatus is disclosed which verifies a program to be embedded into a target machine by running the program in an environment which is one of the target machine, an emulator, and a simulator. Each environment includes operation state information of the program and inputs and outputs the operation state information in a form unique to the environment. The debugging apparatus includes: target environment storing unit for storing an identification name of the target environment; receiving unit for receiving a command from an operator; instruction detecting unit for detecting a certain instruction in the command; specifying unit for, when the certain instruction is detected, specifying a target environment specified by the identification name as a source target environment and for specifying any of the rest of the environments as a destination target environment; reading unit for reading operation state information from the source target environment; converting unit for converting the operation state information into operation state information written in a form unique to the destination target environment; setting unit for setting the converted operation state information in the destination target environment; and operation resuming unit for resuming the operation of the program in the destination target environment.
ABSTRACT WORD COUNT: 199
NOTE:
Figure number on first page: NONE

LEGAL STATUS (Type, Pub Date, Kind, Text):

Examination:	000712	A1	Date of dispatch of the first examination report: 20000531
Application:	971229	A1	Published application (A1with Search Report ;A2without Search Report)
Oppn None:	020123	B1	No opposition filed: 20011101
Grant:	010131	B1	Granted patent
Examination:	980422	A1	Date of filing of request for examination: 980219
Change:	980909	A1	Designated Contracting States (change)

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200105	2391
CLAIMS B	(German)	200105	2162
CLAIMS B	(French)	200105	2762
SPEC B	(English)	200105	13079
Total word count - document A			0
Total word count - document B			20394
Total word count - documents A + B			20394

14/5/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00711606
Start code detector for image sequences
Detektor fur den Startcode von Bildsequenzen
Detecteur de code de depart pour sequences d'images
PATENT ASSIGNEE:
DISCOVISION ASSOCIATES, (260273), 2355 Main Street Suite 200, Irvine, CA 92714, (US), (Proprietor designated states: all)
INVENTOR:

Wise, Adrian Philip, 1[redacted]estbourne Cottages, Frenchay, [redacted]tol BS16 1NA, (GB)
Sotheran, Martin William, The Ridings, Wick Lane, Stinchcombe, Dursley, Gloucestershire GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-Under-Edge, Gloucester. GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 674443 A2 950927 (Basic)
EP 674443 A3 951213
EP 674443 A3 981223
EP 674443 B1 010509
APPLICATION (CC, No, Date): EP 95301301 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED DIVISIONAL NUMBER(S) - PN (AN):
EP 891089 (EP 98202149)
(EP 98202154)
EP 884910 (EP 98202132)
EP 891088 (EP 98202133)
EP 897244 (EP 98202134)
EP 901286 (EP 98202135)
EP 901287 (EP 98202166)
EP 896473 (EP 98202170)
EP 896474 (EP 98202171)
EP 896476 (EP 98202174)
EP 896475 (EP 98202172)
INTERNATIONAL PATENT CLASS: H04N-007/24; **G06F-013/00** ; **G06F-009/38**
CITED PATENTS (EP B): EP 288219 A; EP 460751 A; EP 506294 A; EP 551672 A; EP 572263 A; EP 572766 A; EP 576749 A; EP 577329 A; EP 602621 A; WO 94/25935 A; GB 2269070 A; US 4622585 A; US 4823201 A; US 5173695 A; US 5253053 A
CITED REFERENCES (EP B):
KUN-MIN YANG ET AL: "VLSI ARCHITECTURE DESIGN OF A VERSATILE VARIABLE LENGTH DECODING CHIP FOR REAL-TIME VIDEO CODECS" PROCEEDINGS OF THE REGION 10 CONFERENCE ON COMPUTER AND COMMUNICATI SYSTEMS (TENCON), HONG KONG, 24 - 27 SEPT., 1990, vol. 2, 24 September 1990, pages 551-554, XP000235934 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS
KOMORI S ET AL: "AN ELASTIC PIPELINE MECHANISM BY SELF-TIMED CIRCUITS" IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 23, no. 1, February 1988, pages 111-117, XP000051576
KAORU UCHIDA ET AL: "A PIPELINED DATAFLOW DATAFLOW PROCESSOR ARCHITECTURE BASED ON A VARIABLE LENGTH TOKEN CONCEPT" ARCHITECTURE, UNIVERSITY PARK, AUG. 15 - 19, 1988, vol. 1, 15 August 1988, pages 209-216, XP000079309 BRIGGS F A
TOKUMICHI MURAKAMI ET AL: "A DSP ARCHITECTURAL DESIGN FOR LOW BIT-RATE MOTION VIDEO CODEC" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, vol. 36, no. 10, 1 October 1989, pages 1267-1274, XP000085313
ELLIOTT J A ET AL: "REAL-TIME SIMULATION OF VIDEOPHONE IMAGE CODING ALGORITHMS ON RECONFIGURABLE MULTICOMPUTERS" IEE PROCEEDINGS E. COMPUTERS & DIGITAL TECHNIQUES, vol. 139, no. 3 PART E, 1 May 1992, pages 269-279, XP000306411
MAYER A C: "THE ARCHITECTURE OF A SINGLE-CHIP PROCESSOR ARRAY FOR VIDEOCOMPRESSION" PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON CONSUMER ELECTRONICS, ROSEMONT, JUNE 8 - 10, 1993, no. CONF. 12, 8 June 1993, page 294/295 XP000427624 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS
YONG M CHONG: "A DATA-FLOW ARCHITECTURE FOR DIGITAL IMAGE PROCESSING" WESCON CONFERENCE RECORD,1 January 1984, pages 4/6 1-4/6 10, XP000565437;

ABSTRACT EP 674443 A2
A multi-standard video decompression apparatus has a plurality of stages interconnected by a two-wire interface arranged as a pipeline

processing machine. Control tokens and DATA Tokens pass over the single two-wire interface for carrying both control and data in token format. A token decode circuit is positioned in certain of the stages for recognizing certain of the tokens as control tokens pertinent to that stage and for passing unrecognized control tokens along the pipeline. Reconfiguration processing circuits are positioned in selected stages and are responsive to a recognized control token for reconfiguring such stage to handle an identified DATA Token.

ABSTRACT WORD COUNT: 102

NOTE:
Figure number on first page: 61

LEGAL STATUS (Type, Pub Date, Kind, Text):

Grant:	010509	B1	Granted patent
Application:	950927	A2	Published application (A1with Search Report ;A2without Search Report)
Oppn None:	020502	B1	No opposition filed: 20020212
Lapse:	020403	B1	Date of lapse of European Patent in a contracting state (Country, date): AT 20010509, BE 20010509,
Lapse:	020320	B1	Date of lapse of European Patent in a contracting state (Country, date): BE 20010509,
Lapse:	020410	B1	Date of lapse of European Patent in a contracting state (Country, date): AT 20010509, BE 20010509, CH 20010509, LI 20010509,
Search Report:	951213	A3	Separate publication of the European or International search report
*Search Report:	960110	A2	Separate publication of European or Intl search report (change)
Change:	971022	A2	Representative (change)
Change:	980304	A2	Obligatory supplementary classification (change)
Examination:	981104	A2	Date of filing of request for examination: 980908
Search Report:	981223	A3	Separate publication of the European or International search report
Examination:	990324	A2	Date of despatch of first examination report: 990208

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB95	2897
CLAIMS B	(English)	200119	647
CLAIMS B	(German)	200119	609
CLAIMS B	(French)	200119	752
SPEC A	(English)	EPAB95	128616
SPEC B	(English)	200119	122384
Total word count - document A			131543
Total word count - document B			124392
Total word count - documents A + B			255935

14/5/5 (Item 5 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00711605

Reconfigurable data processing stage

Rekonfigurierbare Datenverarbeitungsstufe

Etage d'operation de donnees reconfigurable

PATENT ASSIGNEE:

DISCOVISION ASSOCIATES, (260273), 2355 Main Street Suite 200, Irvine, CA 92714, (US), (Proprietor designated states: all)

INVENTOR:

Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol, BS16 1NA, (GB)

Sotheran, Martin Willi[redacted] The Ridings, Wick Lane, Stinc[redacted]be, Dursley, Gloucestershire, GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, Gloucestershire, GL11 5PE, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 674446 A2 950927 (Basic)
EP 674446 A3 960814
EP 674446 B1 010801
APPLICATION (CC, No, Date): EP 95301300 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
INTERNATIONAL PATENT CLASS: H04N-007/24; **G06F-013/00** ; **G06F-009/38**
CITED PATENTS (EP B): EP 572766 A; EP 576749 A; WO 94/25935 A
CITED REFERENCES (EP B):
ARCHITECTURE, UNIVERSITY PARK, AUG. 15 - 19, 1988, vol. 1, 15 August 1988, BRIGGS F A, pages 209-216, XP000079309 KAORU UCHIDA ET AL: "A PIPELINED DATAFLOW DATAFLOW PROCESSOR ARCHITECTURE BASED ON A VARIABLE LENGTH TOKEN CONCEPT"
IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 23, no. 1, pages 111-117, XP000051576 KOMORI S ET AL: "AN ELASTIC PIPELINE MECHANISM BY SELF-TIMED CIRCUITS"
IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, vol. 36, no. 10, 1 October 1989, pages 1267-1274, XP000085313 TOKUMICHI MURAKAMI ET AL: "A DSP ARCHITECTURAL DESIGN FOR LOW BIT-RATE MOTION VIDEO CODEC"
IEE PROCEEDINGS E. COMPUTERS & DIGITAL TECHNIQUES, vol. 139, no. 3 PART E, 1 May 1992, pages 269-279, XP000306411 ELLIOTT J A ET AL: "REAL-TIME SIMULATION OF VIDEOPHONE IMAGE CODING ALGORITHMS ON RECONFIGURABLE MULTICOMPUTERS"
PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON CONSUMER ELECTRONICS, ROSEMONT, JUNE 8 - 10, 1993, no. CONF. 12, 8 June 1993, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, page 294/295 XP000427624 MAYER A C: "THE ARCHITECTURE OF A SINGLE-CHIP PROCESSOR ARRAY FOR VIDEOCOMPRESSION"
4TH INTERNATIONAL CONFERENCE ON SIGNAL PROCESSING APPLICATIONS & TECHNOLOGY, vol. 2, 28 September 1993 - 1 October 1993, SANTA CLARA, CALIFORNIA, US, pages 1031-1038, XP002014370 TOM KOPET: "Programmable architectures for real-time video compression"
WESCON '84 CONFERENCE RECORD, ANAHEIM, CA, USA, 30 October 1984 - 1 November 1984, pages 4.6.1-4.6.10, XP002014371 Y.M.CHONG: "A Data-Flow Architecure for Digital Image Processing";

ABSTRACT EP 674446 A3
A multi-standard video decompression apparatus has a plurality of stages interconnected by a two-wire interface arranged as a pipeline processing machine. Control tokens and DATA Tokens pass over the single two-wire interface for carrying both control and data in token format. A token decode circuit is positioned in certain of the stages for recognizing certain of the tokens as control tokens pertinent to that stage and for passing unrecognized control tokens along the pipeline. Reconfiguration processing circuits are positioned in selected stages and are responsive to a recognized control token for reconfiguring such stage to handle an identified DATA Token. A wide variety of unique supporting subsystem circuitry and processing techniques are disclosed for implementing the system. (see image in original document)
ABSTRACT WORD COUNT: 144
NOTE:
Figure number on first page: 10

LEGAL STATUS (Type, Pub Date, Kind, Text):

Grant:	010801	B1	Granted patent
Application:	950927	A2	Published application (A1with Search Report ;A2without Search Report)
Oppn None:	020724	B1	No opposition filed: 20020503
Lapse:	020410	B1	Date of lapse of European Patent in a contracting state (Country, date): AT 20010801,

Lapse:	020717	Date of lapse of European Pat in a contracting state (Country, date): AT 20010801, BE 20010801,
Change:	960501 A2	International patent classification (change)
Change:	960501 A2	Obligatory supplementary classification (change)
Search Report:	960814 A3	Separate publication of the European or International search report
Examination:	970409 A2	Date of filing of request for examination: 970212
Change:	971105 A2	Representative (change)
Examination:	990901 A2	Date of dispatch of the first examination report: 19990713

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB95	2475
CLAIMS B	(English)	200131	1079
CLAIMS B	(German)	200131	1072
CLAIMS B	(French)	200131	1186
SPEC A	(English)	EPAB95	125236
SPEC B	(English)	200131	121335
Total word count - document A			127738
Total word count - document B			124672
Total word count - documents A + B			252410

14/5/6 (Item 6 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00662095
Displaying graphic data.
Darstellung von graphischen Daten.
Affichage de donnees graphiques.
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
Massimo, Messina, Via S. Costanza, 46, I-00198 Roma, (IT)
LEGAL REPRESENTATIVE:
Lettieri, Fabrizio et al (59683), IBM Semea S.p.A. Direzione Brevetti - MI VIM 900 Casella Postale 37 Via Lecco, 61, I-20059 Vimercate (MI), (IT)
PATENT (CC, No, Kind, Date): EP 636965 A1 950201 (Basic)
APPLICATION (CC, No, Date): EP 93110688 930705;
PRIORITY (CC, No, Date): EP 93110688 930705
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: **G06F-003/033** ; G09G-001/16

ABSTRACT EP 636965 A1
A method and system for the management of graphs comprised of a high number of points without affecting the readability of the graph itself. The method and system also allow to keep in the computer memory a number of points greater than the number of points that can be shown in the assigned screen region.
Scrolling functions operate only on the part of the chart representing the data, without the involvement of other portions like legends, titles, scales, descriptions. (see image in original document)
ABSTRACT WORD COUNT: 86

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	950201 A1	Published application (A1with Search Report ;A2without Search Report)
Examination:	950719 A1	Date of filing of request for examination: 950519
Change:	951227 A1	Representative (change)
Withdrawal:	960807 A1	Date on which the European patent application

was withdrawn: 960611
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF2	516
SPEC A	(English)	EPABF2	2254
Total word count - document A			2770
Total word count - document B			0
Total word count - documents A + B			2770

14/5/7 (Item 7 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00562885
Method and system for avoiding selector loads.
Verfahren und System zur Vermeidung von Selektorladungen.
Procede et systeme pour eviter des chargements de selecteur.
PATENT ASSIGNEE:
MICROSOFT CORPORATION, (749861), One Microsoft Way, Redmond, Washington 98052-6399, (US), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
Willman, Bryan M., 10117 N.E. 64th Street, Kirkland, Washington 98033, (US)
LEGAL REPRESENTATIVE:
Patentanwalte Grunecker, Kinkeldey, Stockmair & Partner (100721), Maximilianstrasse 58, D-80538 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 557908 A2 930901 (Basic)
EP 557908 A3 950118
APPLICATION (CC, No, Date): EP 93102677 930219;
PRIORITY (CC, No, Date): US 843994 920226
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: **G06F-012/02 ; G06F-012/10**

ABSTRACT EP 557908 A2
An improved method and system for reducing the number of segment register loads that occur during the transfer of control from an application program to an operating system routine is provided. In preferred embodiments on an Intel 80386 processor, an application program and operating system kernel share a code segment address space and a data segment address space from 0 to 4G. During the execution of the application program, which executes in user mode, a page table is defined to prevent the application program from accessing pages which correspond to the address space of 2G to 4G. When the application program invokes a system routine, the system routine does not need to load the data segment register since the application program and the kernel share the same data segment. If an application program does load the data segment register with a selector other than the selector for the shared data segment, then when the kernel tries to access memory using the data segment register, an exception is generated. The exception handler restores the selector for the shared data segment into the data segment register and resumes execution of the instruction which caused the exception. (see image in original document)
ABSTRACT WORD COUNT: 201

LEGAL STATUS (Type, Pub Date, Kind, Text):

Withdrawal:	20000209 A2	Date application deemed withdrawn: 19990721
Application:	930901 A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	950118 A3	Separate publication of the European or International search report
Examination:	950906 A2	Date of filing of request for examination: 950711
Examination:	980819 A2	Date of despatch of first examination report: 980706

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	1406
SPEC A	(English)	EPABF1	5313
Total word count - document A			6719
Total word count - document B			0
Total word count - documents A + B			6719

14/5/8 (Item 8 from file: 348)

00306062

Digital data processing system.
Digitales Datenverarbeitungssystem.
Systeme du traitement de donnees numeriques.

PATENT ASSIGNEE:
DATA GENERAL CORPORATION, (410940), Route 9, Westboro Massachusetts 01581, (US), (applicant designated states: AT;BE;CH;DE;FR;GB;IT;LI;LU;NL;SE)
INVENTOR:
Bratt, Richard Glenn, 9 Brook Trail Road, Wayland Massachusetts 01778, (US)
Clancy, Gerald F., 13069 Jaccaranda Center, Saratoga California 95070, (US)
Gavrin, Edward S., Beaver Pond Road RFD 4, Lincoln Massachusetts 01773, (US)
Gruner, Ronald Hans, 112 Dublin Wood Drive, Cary North Carolina 27514, (US)
Mundie, Craig James, 136 Castlewood Drive, Cary North Carolina, (US)
Schleimer, Stephen I., 1208 Ellen Place, Chapel Hill North Carolina 27514, (US)
Wallach, Steven J., 12436 Green Meadow Lane, Saratoga California 95070, (US)
LEGAL REPRESENTATIVE:
Robson, Aidan John et al (69471), Reddie & Grose 16 Theobalds Road, London WC1X 8PL, (GB)

PATENT (CC, No, Kind, Date): EP 300516 A2 890125 (Basic)
EP 300516 A3 890426
EP 300516 B1 931124
APPLICATION (CC, No, Date): EP 88200921 820521;
PRIORITY (CC, No, Date): US 266413 810522; US 266539 810522; US 266521 810522; US 266415 810522; US 266409 810522; US 266424 810522; US 266421 810522; US 266404 810522; US 266414 810522; US 266532 810522; US 266403 810522; US 266408 810522; US 266401 810522; US 266524 810522
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IT; LI; LU; NL; SE
RELATED PARENT NUMBER(S) - PN (AN):
EP 67556 (EP 823025960)
INTERNATIONAL PATENT CLASS: **G06F-009/46** ; **G06F-012/14**

CITED REFERENCES (EP A):
PROCEEDINGS OF THE SPRING JOINT COMPUTER CONFERENCE, Atlantic City, 1972, pages 417-429, Afips Press; G.S. GRAHAM et al.: "Protection-Principles and practice"
IDEM.
COMPCON SPRING'80, digest of papers, San Francisco, 25th-28th February 1980, pages 340-343, IEEE, New York, US; T.D. McCREERY: "The X-tree operating system: Bottom layer"
IDEM.
COMPUTER ARCHITECTURE NEWS, October 1980, pages 4-11; J. RATTNER et al.: "Object-based computer architecture"
A.S. TANENBAUM: "Structured computer organization", 1976, pages 264-268, Prentice-Hall, Inc., Englewood Cliffs, New Jersey, US
IBM TECHNICAL DISCLOSURE BULLETIN, vol. 22, no. 3, August 1979, pages 1286-1289, New York, US; D.B. LOMET: "Regions for controlling the propagation of addressability in capability systems";

ABSTRACT EP 300516 A2
The system has memory storing data and instructions and processing means. Memory is organized into objects identified by unique identifiers

(UIDs) comprising a lo[redacted]al allocation unit identifier [redacted]UID) and an object serial number (OSN) provided by an architectural clock, associated with an offset (O) and length (L) enabling logical addresses to be derived. Instructions (SIN's) are in an intermediate level language - (SOP's = S - language operations). Associated names (NAME A, NAME B) point to name tables which identify subjects to which the processor may respond in relation to the instruction in question. Protection is afforded by restricting access to memory operations to a subject pertaining to the set of subjects pertaining to the object in question.

ABSTRACT WORD COUNT: 122

LEGAL STATUS (Type, Pub Date, Kind, Text):

Lapse:	20000209	B1	Date of lapse of European Patent in a contracting state (Country, date): AT 19931124, BE 19931124, FR 19940415, IT 19931124, LU 19940531, NL 19931124, SE 19931124,
Application:	890125	A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	890426	A3	Separate publication of the European or International search report
Examination:	891206	A2	Date of filing of request for examination: 891011
Examination:	920115	A2	Date of despatch of first examination report: 911202
Grant:	931124	B1	Granted patent
Lapse:	940713	B1	Date of lapse of the European patent in a Contracting State: SE 931124
Lapse:	940810	B1	Date of lapse of the European patent in a Contracting State: AT 931124, SE 931124
Change:	940810	B1	Representative (change)
Lapse:	940928	B1	Date of lapse of the European patent in a Contracting State: AT 931124, NL 931124, SE 931124
Oppn None:	941117	B1	No opposition filed
Lapse:	941130	B1	Date of lapse of the European patent in a Contracting State: AT 931124, BE 931124, NL 931124, SE 931124
Lapse:	950118	B1	Date of lapse of the European patent in a Contracting State: AT 931124, BE 931124, FR 940415, NL 931124, SE 931124
Lapse:	991020	B1	Date of lapse of European Patent in a contracting state (Country, date): AT 19931124, BE 19931124, FR 19940415, IT 19931124, NL 19931124, SE 19931124,

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	1018
CLAIMS B	(German)	EPBBF1	868
CLAIMS B	(French)	EPBBF1	1115
SPEC B	(English)	EPBBF1	154256
Total word count - document A			0
Total word count - document B			157257
Total word count - documents A + B			157257

14/5/9 (Item 9 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00306058
Digital data processing system.
Digitales Datenverarbeitungssystem.
Systeme de traitement de donnees numeriques.
PATENT ASSIGNEE:
DATA GENERAL CORPORATION, (410940), Route 9, Westboro Massachusetts 01581

, (US), (applicant designated states: AT;BE;CH;DE;FR;GB;IT;LI;LU;NL;SE)
INVENTOR:
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Wallach, Walter, A., Jr., 1336 Medfield Road, Raleigh North Carolina 27607, (US)
LEGAL REPRESENTATIVE:
Robson, Aidan John et al (69471), Reddie & Grose 16 Theobalds Road, London WC1X 8PL, (GB)
PATENT (CC, No, Kind, Date): EP 290111 A2 881109 (Basic)
EP 290111 A3 890503
EP 290111 B1 931222
APPLICATION (CC, No, Date): EP 88200917 820521;
PRIORITY (CC, No, Date): US 266404 810522
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IT; LI; LU; NL; SE
RELATED PARENT NUMBER(S) - PN (AN):
EP 67556 (EP 823025960)
INTERNATIONAL PATENT CLASS: **G06F-009/30**
CITED PATENTS (EP A): US 3902163 A
CITED REFERENCES (EP A):
COMPUTER ARCHITECTURE NEWS, October 1980, pages 4-11; J. RATTNER et al.: "Object-based computer architecture"
DIGEST OF PAPERS, COMPCON SPRING 1980, 20TH IEEE COMPUTER SOCIETY INTERNATIONAL CONFERENCE, San Francisco, California, 25th-28th February 1980, pages 340-343, IEEE, New York, US; T.D. McCREERY; "The X-tree operating system: bottom layer"
PROCEEDINGS OF THE SPRING JOINT COMPUTER CONFERENCE, 1972, pags 417-429, Afips Press, Atlantic City, N.J., US; G. SCOTT GRAHAM et al.: "Protection - Principles and practice";

ABSTRACT EP 290111 A2
A digital computer system has a memory system organized into objects (10213) for storing items of information and a processor for processing data in response to instructions. An object identifier code is associated with each object. The objects include procedure objects (10312, 10314, 10316) and data objects. The procedure objects contain procedures including the instructions (10344) and name tables (10350) associated with the procedures. The instructions contain operation codes and names representing data. Each name corresponds to a name table entry in the name table (10350) associated with the procedure. The name table for a name contains information from which the processor may determine the location and the format for the data (e.g. an operand) represented by the name.
ABSTRACT WORD COUNT: 123

LEGAL STATUS (Type, Pub Date, Kind, Text):

Lapse:	200002[redacted]B1	Date of lapse of European P[redacted]t in a contracting state (Country, date): AT 19931222, BE 19931222, FR 19940513, IT 19931222, LU 19940531, NL 19931222, SE 19931222,
Application:	881109 A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	890503 A3	Separate publication of the European or International search report
Examination:	891220 A2	Date of filing of request for examination: 891026
Examination:	920115 A2	Date of despatch of first examination report: 911202
Grant:	931222 B1	Granted patent
Change:	940810 B1	Representative (change)
Lapse:	940928 B1	Date of lapse of the European patent in a Contracting State: NL 931222
Lapse:	941026 B1	Date of lapse of the European patent in a Contracting State: NL 931222, SE 931222
Lapse:	941117 B1	Date of lapse of the European patent in a Contracting State: AT 931222, NL 931222, SE 931222
Lapse:	941130 B1	Date of lapse of the European patent in a Contracting State: AT 931222, BE 931222, NL 931222, SE 931222
Oppn None:	941214 B1	No opposition filed
Lapse:	950118 B1	Date of lapse of the European patent in a Contracting State: AT 931222, BE 931222, FR 940513, NL 931222, SE 931222
Lapse:	991020 B1	Date of lapse of European Patent in a contracting state (Country, date): AT 19931222, BE 19931222, FR 19940513, IT 19931222, NL 19931222, SE 19931222,

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	1044
CLAIMS B	(German)	EPBBF1	890
CLAIMS B	(French)	EPBBF1	1185
SPEC B	(English)	EPBBF1	154314
Total word count - document A			0
Total word count - document B			157433
Total word count - documents A + B			157433

14/5/10 (Item 10 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00296266
Failing resource manager in a multiplex communication system.
Verwaltung einer defekten Hilfsquelle in einem Multiplex-Kommunikationssyst em.
Gestion d'une ressource defectueuse dans un systeme de communication a multiplexage.
PATENT ASSIGNEE:
ROLM Systems, (1352641), 4900 Old Ironsides Drive, Santa Clara, CA 95054, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Wah-Ling Breu, Wendy, 211 Thompson Square, Mt. View, CA 94043, (US)
LEGAL REPRESENTATIVE:
Fuchs, Franz-Josef, Dr.-Ing. et al (3891), Postfach 22 13 17, W-8000 Munchen 22, (DE)
PATENT (CC, No, Kind, Date): EP 310782 A2 890412 (Basic)
EP 310782 A3 900627
EP 310782 B1 930310
APPLICATION (CC, No, Date): EP 88112794 880805;
PRIORITY (CC, No, Date): US 105771 871005

DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: H04M-003/22; H04Q-011/04; H04L-012/26; **G06F-011/00**
CITED PATENTS (EP A): US 4260859 A; GB 1123282 A
CITED REFERENCES (EP A):
INTERNATIONAL SWITCHING SYMPOSIUM, 15th - 20th March 1987, Phoenix, Arizona, US; Y. KOSEKI et al.: "SHOOTX: A multiple knowledge based diagnosis expert system for NEAX61 ESS", pages C1.6.1.-C1.6.5. or 0078/0082
ELECTRICAL COMMUNICATION, vol. 60, no. 2, 1986; M. THANDASSERI: "Expert systems application for TXE4A exchanges", pages 154-161;

ABSTRACT EP 310782 A2
A method and apparatus for detecting and analyzing errors in a communications system is described. The method employs expert system techniques to isolate failures to specific field replaceable units and attempts to restore the failing unit to service by removing it from service, resetting the resource and returning it to service if it passes retesting. The expert system techniques include detailed decision trees designed for each resource in the system. The decision trees also filter extraneous sources of errors from affecting the error analysis results.

ABSTRACT WORD COUNT: 89
LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	890412	A2	Published application (A1with Search Report ;A2without Search Report)
Examination:	891004	A2	Date of filing of request for examination: 890809
Search Report:	900627	A3	Separate publication of the European or International search report
Change:	911106	A2	Representative (change)
*Assignee:	911106	A2	Applicant (transfer of rights) (change): ROLM Systems (1352641) 4900 Old Ironsides Drive Santa Clara, CA 95054 (US) (applicant designated states: DE;FR;GB)
*Assignee:	911106	A2	Previous applicant in case of transfer of rights (change): International Business Machines Corporation (200120) Old Orchard Road Armonk, N.Y. 10504 (US) (applicant designated states: DE;FR;GB)
Examination:	920722	A2	Date of despatch of first examination report: 920611
Grant:	930310	B1	Granted patent
Oppn None:	940302	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPABF1	892
SPEC B	(English)	EPABF1	36667
Total word count - document A			0
Total word count - document B			37559
Total word count - documents A + B			37559

14/5/11 (Item 11 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00259267
Fast point/line correlations in graphic entities.
Schnelle Punkt-/Zeilenkorrelationen in graphischen Gebilden.
Correlations rapides de points/lignes dans des entites graphiques.
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Reynolds, David Corder, 6200 Habitat Drive Apt. 1053, Boulder, Co 80301, (US)

Wong, Michael Nmi, 3924 Wedge Court, Longmont Colorado 80501, (US)
LEGAL REPRESENTATIVE:
Schuffenecker, Thierry (69981), Compagnie IBM France, Departement de Propriete Intellectuelle, F-06610 La Gaude, (FR)
PATENT (CC, No, Kind, Date): EP 272379 A2 880629 (Basic)
EP 272379 A3 901227
EP 272379 B1 940518
APPLICATION (CC, No, Date): EP 87112938 870904;
PRIORITY (CC, No, Date): US 926485 861103
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: **G06F-003/033**
CITED PATENTS (EP A): EP 82904 A; EP 203324 A

ABSTRACT EP 272379 A2
Graphics display system having a moving cursor, such as a cursor, for selecting a displayed entity with the capability of determining which one of several lower level entities in the vicinity of the cursor is to be selected. The correlation of a cursor with a entity intended to be selected is performed by calculating an index that does not represent the actual distance, which is time consuming, but rather represents a value, more quickly calculated, such that the size order among the indices is the same as the size order of the distances they represent.
ABSTRACT WORD COUNT: 99

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	880629 A2	Published application (A1with Search Report ;A2without Search Report)
Examination:	881102 A2	Date of filing of request for examination: 880910
Search Report:	901227 A3	Separate publication of the European or International search report
Change:	901227 A2	International patent classification (change)
Examination:	931013 A2	Date of despatch of first examination report: 930831
Grant:	940518 B1	Granted patent
Oppn None:	950510 B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	521
CLAIMS B	(German)	EPBBF1	524
CLAIMS B	(French)	EPBBF1	558
SPEC B	(English)	EPBBF1	3540
Total word count - document A			0
Total word count - document B			5143
Total word count - documents A + B			5143

14/5/12 (Item 12 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00874788 **Image available**
UNIFIED TRUST MODEL PROVIDING SECURE IDENTIFICATION, AUTHENTICATION AND VALIDATION OF PHYSICAL PRODUCTS AND ENTITIES, AND PROCESSING, STORAGE, AND EXCHANGE OF INFORMATION
MODELE VALIDE UNIQUE PERMETTANT L'IDENTIFICATION, L'AUTHENTIFICATION ET LA VALIDATION SECURISEES DE PRODUITS ET D'ENTITES PHYSIQUES, ET TRAITEMENT, ENREGISTREMENT ET ECHANGE D'INFORMATIONS
Patent Applicant/Assignee:
AUTHENTISURE INC, 2455 Sawgrass Court, Fairfield, CA 94533, US, US (Residence), US (Nationality)
Inventor(s):
SALOMON Allen, 2465 Sawgrass Court, Fairfield, CA 94533, US,
TRINKA Roland, 667 Northern Avenue, Mill Valley, CA 94941, US,
Legal Representative:
BINGHAM Marcel (et al) (agent), Hickman Palermo Truong & Becker, LLP, 1600 Willow Street, San Jose, CA 95125, US,

Patent and Priority Information (Country, Number, Date):
  Patent: WO 200208875 A2 20020131 (WO 0208875)
  Application: WO 2001US23398 20010725 (PCT/WO US0123398)
  Priority Application: US 2000221221 20000725
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU
  CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP
  KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD
  SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
  (EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
  (OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
  (AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
  (EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-001/00**
Publication Language: English
Filing Language: English
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 14780

English Abstract
  A security infrastructure is described that enables a high secure, dynamic, robust, and extensible security infrastructure. The security infrastructure uses integrated circuits (TEIs) that generate a unique set of output values in response to receiving a given set of "input seed values". The particular output values generated by a TEI in response to input seed values cannot, for all practical purposes, be predicted. "Trusted Objects" (TOs) are data structures that are encrypted using keys generated from the unique set of output values generated by one or mroe TEIs in response to input seed values applied to those TEIs. The keys are formed using a key generation process that computes keys from the TEI output values. Thus, the keys may be regenerated by later applying the same input seed values to the TEIs, and applying the resultant output values to the key generation process to reproduce the original keys.

French Abstract
  La presente invention concerne une infrastructure de securite permettant d'obtenir une infrastructure de securite hautement securisee, dynamique, robuste et extensible. L'infrastructure de securite fait intervenir l'utilisation de circuits integres (TEI) qui produisent un ensemble unique de valeurs de sortie en reponse a la reception d'un ensemble donne de valeurs d'entree de depart ("input seed values"). Les valeurs de sortie particulieres produites par un TEI en reponse a des valeurs d'entree de depart ne peuvent pas, a toutes fins pratiques, etre prevues. Des objets valides ("Trusted Objects" / TO) sont des structures qui sont codees au moyen de cles produites a partir de l'ensemble unique de valeurs de sortie produites par le(s) TEI en reponse aux valeurs d'entree de depart appliquees a ces TEI. Les cles sont constituees au moyen d'un processus de production de cles qui determine des cles a partir des valeurs de sortie de TEI. Ainsi, les cles peuvent etre produites par ce dernier par application des memes valeurs d'entree de depart aux TEI, et par application des valeurs de sortie resultantes au processus de production de cles afin de produire des cles uniques.

Legal Status (Type, Date, Text)
Publication 20020131 A2 Without international search report and to be republished upon receipt of that report.
Examination 20020906 Request for preliminary examination prior to end of 19th month from priority date

14/5/13 (Item 13 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00857190 **Image available**
A NETWORK DEVICE FOR SUPPORTING MULTIPLE UPPER LAYER NETWORK PROTOCOLS OVER A SINGLE NETWORK CONNECTION

DISPOSITIF DE RESEAU COMPATIBLE AVEC PLUSIEURS PROTOCOLES DE RESEAU A COUCHE SUPERIEURE VIA UNE SEULE CONNEXION RESEAU

Patent Applicant/Assignee:
EQUIPE COMMUNICATIONS CORPORATION, 100 Nagog Park, Acton, MA 01720, US, US (Residence), US (Nationality)
Inventor(s):
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PERRY Thomas R, 230 Hayden Road, Groton, MA 01450, US,
KIDDER Joseph D, 31 Bonad Road, Arlington, MA 02476, US,
SULLIVAN Daniel J, 35 Glen Road, Hopkinton, MA 01748, US,
FOX Barbara A, 67 Eliot Park, Arlington, MA 02474, US,
MADSEN Jonathon D, 34 Park Avenue Extn., Arlington, MA 02474, US,
PROVENCHER Roland T, 28 Richman Road, Hudson, NH 03051, US,
PEARSON Terrence S, 8 Hills Farm Lane, Hollis, NH 03049, US,
BHATT Umesh, 26 Brackenwood Drive, Nashua, NH 03062, US,
POTHIER Peter, 54 Maplewood Drive, Townsend, MA 01469, US,
MANOR Larry B, 15 Cross Road, Londonderry, NH 03053, US,
Legal Representative:
ENGELLENNER Thomas J (et al) (agent), Nutter, McClennen & Fish, LLP, One International Place, Boston, MA 02110-2699, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200190843 A2-A3 20011129 (WO 0190843)
Application: WO 2001US15867 20010516 (PCT/WO US0115867)
Priority Application: US 2000574343 20000520; US 2000574341 20000520; US 2000574440 20000520; US 2000588398 20000606; US 2000591193 20000609; US 2000593034 20000613; US 2000596055 20000616; US 2000613940 20000711; US 2000616477 20000714; US 2000625101 20000724; US 2000633675 20000807; US 2000637800 20000811; US 2000653700 20000831; US 2000656123 20000906; US 2000663947 20000918; US 2000669364 20000926; US 2000687191 20001012; US 2000703856 20001101; US 2000711054 20001109; US 2000718224 20001121; US 2001756936 20010109; US 2001777468 20010205; US 2001789665 20010221; US 2001803783 20010312; US 2001832436 20010410
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-013/00**
International Patent Class: **G06F-017/30** ; **G06F-001/18** ; **G06F-011/30** ; **G06F-012/14** ; **G06F-003/14** ; H04L-012/56; H04M-001/10; H04M-007/00; H04M-003/00; H01J-003/14
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 210510

English Abstract
The present invention provides a network device with at least one physical interface or port (44,68) that is capable of transferring network packets including data organized into one or more upper layer network protocols. Network packets are received by the port (44,68) and a port subsystem in accordance with a physical layer network protocol and transferred to forwarding subsystems within the network device in accordance with the upper layer protocols into which the network packets data has been organized. Network packets including data organized in accordance with ATM are then transferred to one or more ATM forwarding subsystems, network packets including data organized in accordance with MPLS are transferred to one or more MPLS forwarding subsystems, and network packets including data organized in accordance with IP are transferred to one or more IP forwarding subsystems.

French Abstract
L'invention concerne un dispositif de reseau comportant au moins une interface ou port physique pouvant transferer des paquets de reseau contenant des donnees organisees en un ou plusieurs protocoles reseau a couche superieure (par exemple, ATM, MPLS, IP, Frame Relay, Voice, Circuit Emulation). Ledit port peut etre connecte a une annexe de reseau afin de permettre que le dispositif de reseau puisse transferer des paquets de reseau avec d'autres dispositifs de reseau. Des paquets de reseau sont recus par le port et un sous-systeme de port conforme a un protocole de reseau a couche physique, puis transferes vers des sous-systemes de reexpedition a l'interieur du dispositif de reseau conformes aux protocoles a couche superieure dans lesquels les donnees de paquets de reseau ont ete organisees. Par exemple, les donnees organisees conformement a ATM via SONET, MPLS via SONET et IP via SONET peuvent etre transferees via une annexe de reseau vers un port du dispositif de reseau. Les paquets de reseau contenant des donnees organisees conformement a ATM sont ensuite transferes vers un ou plusieurs sous-systemes de reexpedition ATM et les paquets de reseau contenant des donnees organisees conformement a IP sont transferes sur un ou plusieurs sous-systemes de reexpedition IP. Pour une efficacite accrue, ce dispositif de reseau permet a l'administrateur de reseau de n'ajouter que le nombre et les types de sous-systemes de reexpedition necessaires pour repondre au service de reseau souscrit pour chaque protocole de reseau a couche. Par ailleurs, ce dispositif de reseau peut necessiter moins d'interfaces physiques que les dispositifs de reseau anterieurs.

Legal Status (Type, Date, Text)
Publication 20011129 A2 Without international search report and to be republished upon receipt of that report.
Search Rpt 20020704 Late publication of international search report
Republication 20020704 A3 With international search report.

14/5/14 (Item 14 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00784185 **Image available**
A SYSTEM AND METHOD FOR STREAM-BASED COMMUNICATION IN A COMMUNICATION SERVICES PATTERNS ENVIRONMENT
SYSTEME, PROCEDE ET ARTICLE DE PRODUCTION FOURNISSANT UN SYSTEME DE COMMUNICATION EN CONTINU DANS UN ENVIRONNEMENT DE CONFIGURATIONS DE SERVICES DE COMMUNICATION
Patent Applicant/Assignee:
ACCENTURE LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US (Residence), US (Nationality)
Inventor(s):
BOWMAN-AMUAH Michel K, 6426 Peak Vista Circle, Colorado Springs, CO 80918, US,
Legal Representative:
HICKMAN Paul L (agent), Hickman Coleman & Hughes, LLP, P.O. Box 52037, Palo Alto, CA 94303-0746, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200117195 A2-A3 20010308 (WO 0117195)
Application: WO 2000US24125 20000831 (PCT/WO US0024125)
Priority Application: US 99386717 19990831
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: H04L-029/06
International Patent Class: **G06F-017/22** ; H04L-029/12
Publication Language: English
Filing Language: English

Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 150532

English Abstract
A system, method, and article of manufacture are disclosed for providing a stream-based communication system. A shared format is defined on interface code for a sending system and a receiving system. A message to be sent from the sending system to the receiving system is translated based on the shared format. Once translated, the message is then sent from the sending system and received by the receiving system. Once the message is received by the receiving system, the message is then translated based on the shared format.

French Abstract
L'invention concerne un systeme, un procede et un article de production fournissant un systeme de communication en continu. Un format partage est defini selon un code d'interface pour un systeme emetteur et un systeme recepteur. Un message devant etre envoye par le systeme emetteur est traduit sur la base du format partage. Une fois traduit, le message est envoye du systeme emetteur et recu par le systeme recepteur. Le message recu par le systeme recepteur est ensuite traduit sur la base du format partage.

Legal Status (Type, Date, Text)
Publication 20010308 A2 Without international search report and to be republished upon receipt of that report.
Examination 20010907 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20011115 Late publication of international search report
Republication 20011115 A3 With international search report.

14/5/15 (Item 15 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00784140
A SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR A GLOBALLY ADDRESSABLE INTERFACE IN A COMMUNICATION SERVICES PATTERNS ENVIRONMENT
SYSTEME, PROCEDE ET ARTICLE DE FABRICATION S'APPLIQUANT DANS UN ENVIRONNEMENT DE STRUCTURE DE SERVICES DE COMMUNICATIONS VIA UNE INTERFACE ADRESSABLE GLOBALEMENT
Patent Applicant/Assignee:
ANDERSEN CONSULTING LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US (Residence), US (Nationality)
Inventor(s):
BOWMAN-AMUAH Michel K, 6426 Peak Vista Circle, Colorado Springs, CO 80918, US,
Legal Representative:
HICKMAN Paul L (agent), Hickman Coleman & Hughes, LLP, P.O. Box 52037, Palo Alto, CA 94303-0746, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200116735 A2 20010308 (WO 0116735)
Application: WO 2000US24198 20000831 (PCT/WO US0024198)
Priority Application: US 99387214 19990831
Designated States: AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CU CZ DE DK DZ EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-009/46**
Publication Language: English
Filing Language: English

Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 150371

English Abstract
  A system, method, and article of manufacture are provided for delivering service via a globally addressable interface. A plurality of interfaces are provided with access allowed to a plurality of different sets of services from each of the interfaces. Each interface has a unique set of services associated therewith. Each of the interfaces is named with a name indicative of the unique set of services associated therewith. The names of the interfaces are then broadcast to a plurality of systems requiring service.

French Abstract
  L'invention porte sur un systeme, un procede et un article de fabrication appliques dans la distribution de services via une interface adressable globalement. Une pluralite d'interfaces permettent d'acceder a une pluralite de differents ensembles de services. A chaque interface est associe un ensemble unique de services. Chacune de ces interfaces est affectee d'un nom designant l'ensemble unique de services correspondant. Les noms des interfaces sont ensuite diffuses a une pluralite de systemes requerant un service.

Legal Status (Type, Date, Text)
Publication 20010308 A2 Without international search report and to be republished upon receipt of that report.
Examination 20010927 Request for preliminary examination prior to end of 19th month from priority date

14/5/16 (Item 16 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00784139
A SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR A SELF-DESCRIBING STREAM IN A COMMUNICATION SERVICES PATTERNS ENVIRONMENT
SYSTEME, PROCEDE ET ARTICLE DE FABRICATION DESTINES A UN FLUX D'AUTODESCRIPTEURS DANS UN ENVIRONNEMENT DE MODELES DE SERVICES DE COMMUNICATION
Patent Applicant/Assignee:
  ACCENTURE LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US (Residence), US (Nationality)
Inventor(s):
  BOWMAN-AMUAH Michel K, 6426 Peak Vista Circle, Colorado Springs, CO 80918, US,
Legal Representative:
  HICKMAN Paul L (agent), Oppenheimer Wolff & Donnelly, LLP, 1400 Page Mill Road, Palo Alto, CA 94304, US,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 200116734 A2-A3 20010308 (WO 0116734)
  Application: WO 2000US23999 20000831 (PCT/WO US0023999)
  Priority Application: US 99387070 19990831
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
  (EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
  (OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
  (AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
  (EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-009/46**
Publication Language: English
Filing Language: English
Fulltext Availability:
  Detailed Description

Claims
Fulltext Word Count: 150517

English Abstract
A system, method, and article of manufacture are described for providing a self-describing stream-based communication system. Messages are sent which include data between a sending system and a receiving system. Meta-data is attached to the messages being sent between the sending system and the receiving system. The data of the messages sent from the sending system to the receiving system is translated based on the meta-data. The meta-data includes first and second sections. The first section identifies a type of object associated with the data and a number of attribute descriptors in the data. The second section includes a series of the attribute descriptors defining elements of the data.

French Abstract
L'invention concerne un systeme, un procede et un article de fabrication destines a constituer un systeme de communication a base d'un flux d'autodescripteurs. Des messages comprenant des donnees sont envoyes, entre un systeme expediteur et un systeme recepteur. Des metadonnees sont attachees aux messages en cours d'envoi entre le systeme expediteur et le systeme recepteur. Les donnees des messages envoyes du systeme expediteur au systeme recepteur sont traduites d'apres les metadonnees, lesquelles comprennent des premiere et seconde sections. La premiere section identifie un type d'objet associe aux donnees et un nombre de descripteurs d'attributs presents dans celles-ci. La seconde section comprend une serie de descripteurs d'attributs definissant des elements des donnees.

Legal Status (Type, Date, Text)
Publication 20010308 A2 Without international search report and to be republished upon receipt of that report.
Examination 20010927 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20020221 Late publication of international search report
Republication 20020221 A3 With international search report.

14/5/17 (Item 17 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00784131
A SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR A MULTI-OBJECT FETCH COMPONENT IN AN INFORMATION SERVICES PATTERNS ENVIRONMENT
SYSTEME, PROCEDE ET ARTICLE MANUFACTURE POUR COMPOSANT DE RECUPERATION MULTI-OBJET DANS UN ENVIRONNEMENT CARACTERISE PAR DES SERVICES D'INFORMATIONS

Patent Applicant/Assignee:
ACCENTURE LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US (Residence), US (Nationality)
Inventor(s):
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Legal Representative:
HICKMAN Paul L (agent), Oppenheimer Wolff & Donnelly LLP, Suite 3800, 2029 Century Park East, Los Angeles, CA 90067, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200116723 A2-A3 20010308 (WO 0116723)
Application: WO 2000US24083 20000831 (PCT/WO US0024083)
Priority Application: US 99386238 19990831
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW

(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-009/44**
International Patent Class: **G06F-009/46**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 150940

English Abstract
A system, method, and article of manufacture are provided for retrieving muliple business objects across a network in one access operation. A business object and a plurality of remaining objects are provided on a persistent store. Upon receiving a request for the business object, it is established which of the remaining objects are related to the business object. The related objects and the business object are retrieved from the persistant store in one operation and it is determined how the retrieved related objects relate to the business object and each other. A graph of relationships of the business and related objects is instantiated in memory.

French Abstract
La presente invention concerne un systeme, un procede et un article manufacture destine a la recuperation de plusieurs objets d'affaires dans un reseau en une operation d'acces. A cet effet, on dispose dans une memoire permanente d'un objet d'affaire et d'une pluralite d'objets restants. Des la reception d'une requete se rapportant a un objet d'affaires, on recherche deux des objets restants qui sont en relations avec l'objet d'affaires. Une seule operation permet ainsi de recuperer dans la memoire permanente ces objets ainsi que l'objet d'affaires. Il ne reste plus qu'a determiner les relations existant d'une part entre les objets consideres et d'autre part entre ces objets et l'objet d'affaires. Une instanciation d'un graphique des relations entre les objets et l'objet d'affaire est conservee en memoire.

Legal Status (Type, Date, Text)
Publication 20010308 A2 Without international search report and to be republished upon receipt of that report.
Examination 20010809 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20020912 Late publication of international search report
Republication 20020912 A3 With international search report.

14/5/18 (Item 18 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00777022
A SYSTEM, METHOD AND ARTICLE OF MANUFACTURE FOR AN E-COMMERCE BASED ARCHITECTURE
SYSTEME, PROCEDE ET ARTICLE DE PRODUCTION POUR UNE ARCHITECTURE BASEE SUR LE COMMERCE ELECTRONIQUE
Patent Applicant/Assignee:
AC PROPERTIES BV, Parkstraat 83, NL-2514 JG 'S Gravenhage, NL, NL (Residence), NL (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
UNDERWOOD Roy A, 4436 Hearthmoor Court, Long Grove, IL 60047, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
HICKMAN Paul L (et al) (agent), Hickman Coleman & Hughes, LLP, P.O. Box 52037, Palo Alto, CA 94303-0746, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200109794 A2-A3 20010208 (WO 0109794)
Application: WO 2000US20704 20000728 (PCT/WO US0020704)
Priority Application: US 99364734 19990730
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES

FI GB GE GH GM HR HU I[redacted] IS JP KE KG KP KR KZ LC LK L[redacted] LT LU LV MD
MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US
UZ VN YU ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: **G06F-009/46**
International Patent Class: **G06F-009/44 ; G06F-017/30 ; G06F-017/60**
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 122424

English Abstract
A system, method and article of manufacture provide a resources e-commerce technical architecture where context objects are shared among a plurality of components executed on a transaction server. Services are also accessed within the server without a need for knowledge of an application program interface of the server. Application consistency is maintained by referencing text phrases throug a short codes framework. Additionally, a graphical user interface is also generated for the resources e-commerce technical architecture.

French Abstract
Un systeme, un procede et un article de production fournissent une architecture technique de commerce electronique a ressources dans laquelle des objets de contexte sont partages parmi une pluralite de constituants executes sur un serveur de transactions. Il est aussi possible d'acceder a des services a l'interieur du serveur sans la necessite d'une connaissance d'une interface de programme d'application du serveur. La coherence des applications est maintenue par reference aux phrases textuelles au moyen d'une structure de codes courts. De plus, une interface utilisateur graphique est egalement generee pour l'architecture technique de commerce electronique a ressources.

Legal Status (Type, Date, Text)
Publication 20010208 A2 Without international search report and to be republished upon receipt of that report.
Search Rpt 20010614 Late publication of international search report
Republication 20010614 A3 With international search report.
Examination 20011101 Request for preliminary examination prior to end of 19th month from priority date

14/5/19 (Item 19 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00300850 **Image available**
UPDATE MECHANISM FOR COMPUTER STORAGE CONTAINER MANAGER
MOYEN DE MISE A JOUR POUR MODULE DE GESTION D'ELEMENTS DE STOCKAGE D'ORDINATEURS
Patent Applicant/Assignee:
APPLE COMPUTER INC,
Inventor(s):
HARRIS Jared M,
RUBEN Ira L,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9519001 A1 19950713
Application: WO 95US196 19950104 (PCT/WO US9500196)
Priority Application: US 94177853 19940105
Designated States: AM AT AU BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU JP KE KG KP KR KZ LK LR LT LU LV MD MG MN MW MX NL NO NZ PL PT RO RU SD SE SI SK TJ TT UA UZ VN KE MW SD SZ AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG

Main International Patent Class: **G06F-009/44**
Publication Language: English
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 119635

English Abstract
Methods and data structures are defined which permit information to be stored as objects in target containers and update containers. A target container defines a first state of the information, and the update container, which can point to the target container, identifies changes to the information in the first state which would be sufficient to update the first information state to a second information state. Update containers may be nested to any depth. When an application program opens an update container, the procedure searches down the chain until it finds the ultimate target container. It then creates in-memory structures for providing access to the objects and value data represented in such container. The procedure then works its way back up the chain, performing the changes on the in-memory structure, which are called for in each of the update containers.

French Abstract
L'invention se rapporte a des structures de donnees et a des procedes permettant de stocker des informations sous forme d'objets dans des elements de stockage cibles et dans des elements de stockage de mise a jour. Un element de stockage cible definit un premier etat relatif aux informations, et l'element de stockage de mise a jour, qui peut identifier l'element de stockage cible, identifie des modifications des informations presentant le premier etat, qui devraient permettre la mise a jour dudit premier etat en un second etat. Les elements de stockage de mise a jour peuvent s'emboiter indefiniment. Lorsqu'un programme d'application ouvre un element de stockage de mise a jour, la procedure appliquee consiste a effectuer une recherche le long de la chaine jusqu'a ce que l'element de stockage cible au bout de la chaine soit identifie. Des structures en memoire sont alors creees afin de permettre l'acces aux objets et aux donnees de valeur representes dans un tel element de stockage. La procedure consiste alors a remonter la chaine, et a effectuer, dans la structure en memoire, les modifications requises dans chacun des elements de stockage de mise a jour.

14/5/20 (Item 20 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00234265 **Image available**
SYSTEM FOR DIVIDING PROCESSING TASKS INTO SIGNAL PROCESSOR AND DECISION-MAKING MICROPROCESSOR INTERFACING
SYSTEME DE SEPARATION DES TACHES DE TRAITEMENT EN TACHES POUR INTERFACAGE AVEC UN PROCESSEUR DE SIGNAUX ET UN MICROPROCESSEUR DE PRISE DE DECISION
Patent Applicant/Assignee:
  STAR SEMICONDUCTOR CORPORATION,
Inventor(s):
  ROBINSON Jeffrey I,
  ROUSE Keith,
  KRASSOWSKI Andrew J,
  MONTLICK Terry F,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 9308524 A1 19930429
  Application: WO 92US8954 19921014 (PCT/WO US9208954)
  Priority Application: US 91776161 19911015
Designated States: AU CA JP KR AT BE CH DE DK ES FR GB GR IE IT LU MC NL SE
Main International Patent Class: **G06F-009/00**
International Patent Class: **G06F-09:40**
Publication Language: English
Fulltext Availability:

Detailed Description
Claims
Fulltext Word Count: 219172

English Abstract
Architectures and methods are provided for efficiently dividing a processing task into tasks for a programmable real time signal processor (SPROC) (10) and tasks for a decision-making microprocessor (2120). The SPROC is provided with a non-interrupt structure where data flow is through a multiported central memory. The SPROC is also programmed in an environment which requires nothing more than graphic entry of a block diagram of the user's design. In automatically implementing the block diagram into silicon, the SPROC programming/development environment accounts for and provides software connection and interfaces with a host microprocessor (2120). The programming environment preferably includes: a high-level computer screen entry system which permits choosing, entry, parameterization, and connection of a plurality of functional blocks; a functional block cell library (2015) which provides source code representing the functional blocks; and a signal processor scheduler/compiler (2040) which uses the functional block cell library (2015) and the information entered into the high-level entry system to compile a program and to output source program code for a program memory and source data code for the data memory of the SPROC, as well as a symbol table which provides a memory map which maps SPROC addresses to variable names which the microprocessor (2120) will refer to in separately compiling its program.

French Abstract
On decrit des architectures et procedes qui permettent de separer efficacement une tache de traitement en taches destinees a un processeur de signaux programmable fonctionnant en temps reel (SPROC)(10) et a un microprocesseur de prise de decision (2120). Le SPROC est dote d'une structure depourvue d'interruption ou le flux de donnees arrive par l'intermediaire d'une memoire centrale a ports multiples. Il est aussi programme dans un environnement n'exigeant rien d'autre que l'introduction graphique d'un schema global relatif aux intentions de l'utilisateur. Avec la realisation automatique du schema global dans le silicium, l'environnement de programmation et de developpement du SPROC prend en compte et fournit la connexion au logiciel et realise une interface avec un microprocesseur hote (2120). Cet environnement de programmation comporte de preference un systeme d'introduction a ecran d'affichage perfectionne qui permet de choisir, introduire, parametriser et fournit une connexion avec differents blocs fonctionnels; une bibliotheque a cellules de bloc fonctionnel (2015) qui fournit un code source representant les blocs fonctionnels; et un programmateur/compileur pour processeur de signal (2040). Ce dernier utilise la bibliotheque a cellules (2015) et l'information introduite dans le systeme d'introduction perfectionne pour compiler un programme et delivrer en sortie un code de programme source concernant une memoire du programme et un code de donnees source destine a la memoire de donnees du SPROC, ainsi qu'une table de symboles qu fournit une cartographie memorisee, contenant les adresses donnees par le SPROC aux differents noms auxquels le microprocesseur (2120) viendra se referer en compilant separement son propre programme.

14/5/21 (Item 21 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00157186
SHOPPERS COMMUNICATION SYSTEM AND PROCESSES RELATING THERETO
SYSTEME DE COMMUNICATIONS POUR ACHETEURS ET PROCEDES S'Y RAPPORTANT
Patent Applicant/Assignee:
VELA Leo,
MARTIN Roger L,
SASSER Thurman,
Inventor(s):

VELA Leo,
MARTIN Roger L,
SASSER Thurman,
Patent and Priority Information (Country, Number, Date):
Patent: WO 8903555 A1 19890420
Application: WO 88US3432 19881006 (PCT/WO US8803432)
Priority Application: US 87437 19871014
Designated States: AT AU BB BE BG BJ BR CF CG CH CM DE DK FI FR GA GB HU IT JP KP KR LK LU MC MG ML MR MW NL NO RO SD SE SN SU TD TG
Main International Patent Class: **G06F-003/02**
International Patent Class: **G06F-03:14**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 32873

English Abstract
A communication system (22) for a marketing area (33) locates a light signal generating system (25) and a master computer (24) at a control center (23) and delivers message bearing light signals over optical channels (61) to predetermined subdivisions of the marketing area. Message relay units (27) are provided on the shopping carts in the marketing area for transmitting audio and/or visual messages to the shopper. The relay units (27) disclosed have a computer (74) which operates under the control of the master computer (24), a signal receiving system (85) and various message signal storage facilities (112) (118) (122) as well as a message transmission system (71) that includes a video display device (72) and an audio transmission device (75). Various computer controls are provided for shopper use, including controls (126) (128) (129) (130) (131) that facilitate the recording of items destined for purchase by the shopper and which facilitate the generation of indicia on the graphics display indicative of the item locations in the marketing area and a control (138) that changes the size and viewing mode of the graphics display of the marketing area.

French Abstract
Un systeme de communication (22) destine a une zone commerciale (33) localise un systeme produisant un signal lumineux (25) ainsi qu'un ordinateur central (24) a un centre de commande (23), et envoie des signaux lumineux porteurs de messages sur des canaux optiques (61) a des subdivisions de la zone commerciale. Des unites de relais de messages (27) sont montees sur les chariots a provisions dans la zone commerciale, afin de transmettre des messages audio et/ou visuels a l'acheteur. Les unites de relais (27) comportent un ordinateur (74) fonctionnant sous la commande de l'ordinateur central (24), un systeme de reception de signaux (85) ainsi que differents dispositifs de stockage de signaux de messages (112) (118) (122), et un systeme (71) de transmission de messages comprenant un dispositif d'affichage video (72), a quoi s'ajoute un dispositif de transmission audio (75). Differentes commandes d'ordinateur sont prevues a l'usage de l'acheteur, comprenant les commandes (126), (128), (129), (130), (131) facilitant l'enregistrement d'articles destines a etre achetes par l'acheteur et la production de signes sur l'affichage graphique, indiquant les emplacements des articles dans la zone commerciale, ainsi qu'une commande (138) changeant la taille et le mode de visualisation de l'affichage graphique de la zone commerciale.

14/5/22 (Item 22 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00143093 **Image available**
COMPUTER AUTOMATED SENSORY AND MOTOR FUNCTION ASSESSMENT
ESTIMATION AUTOMATISEE PAR ORDINATEUR DE FONCTIONS SENSORIELLES ET MOTRICES
Patent Applicant/Assignee:
BOARD OF REGENTS THE UNIVERSITY OF TEXAS SYSTEM,
Inventor(s):

KONDRASKE George V,
Patent and Priority Information (Country, Number, Date):
Patent: WO 8707969 A2 19871230
Application: WO 87US1473 19870622 (PCT/WO US8701473)
Priority Application: US 86110 19860623
Designated States: AT AT AU BB BE BG BJ BR CF CG CH CH CM DE DE DK FI FR GA GB GB HU IT JP KP KR LK LU LU MC MG ML MR MW NL NL NO RO SD SE SE SN SU TD TG
Main International Patent Class: **G06F-015/42**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 18488
English Abstract

Quantitative numerical profiles and graphical displays of human function/performance capabilities are produced from serial measurements derived from a battery of transducers which sense physical parameters in response to a visual, auditory, or mechanical stimulus and/or special task definition. In different aspects, a sufficient, selected subset of available measurements are administered, representative data is obtained and processed to yield one or several characteristic feature measures corresponding to functions such as strength, range of motion, speed, coordination, etc., and the quantitative functional profile is displayed as a formatted array of individual measures. In other aspects, statistical comparison arrays, representing a normalized version of the raw measure array, is generated. This array is used to produce one of several application dependent display formats, or to generate a functional profile visualization, relating combinations of individual normalized array elements directly to human anatomic (body) sites. In other aspects, the normalized array is used in combination with special knowledge and/or data bases to yield application dependent predictions related to various aspects of human performance.

French Abstract

Des profils numeriques quantitatifs et des affichages graphiques de capacites de fonctions/performances humaines sont produites a partir de mesures serielles derivees d'une batterie de transducteurs qui detectent des parametres physiques en reponse a un stimulus visuel, auditif ou mecanique et/ou a une definition d'une tache speciale. Dans differents aspects, un sous-ensemble suffisant et selectionne de mesures disponibles est administre, des donnees representatives sont obtenues et traitees pour produire une ou plusieurs mesures caracteristiques correspondant a des fonctions telles que la resistance, la plage de deplacement, la vitesse, la coordination, etc., et le profil fonctionnel quantitatif est affiche sous la forme d'un reseau formate de mesures individuelles. Dans d'autres aspects, des ensembles de comparaison statistique, representant une version normalisee de l'ensemble de mesures brutes, sont generees. Cet ensemble est utilise pour produire l'un de plusieurs formats d'affichage dependant de l'application, ou pour generer une visualisation d'un profil fonctionnel, mettant en relation des combinaisons d'elements d'ensembles normalises individuels directement avec des sites anatomiques du corps humain. Dans d'autres aspects, l'ensemble normalise est utilise en combinaison avec des bases de connaissances et/ou de donnees speciales pour produire des predictions dependant de l'application relatives a divers aspects des performances humaines.

14/5/23 (Item 23 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00106554 **Image available**
DATA PROCESSING SYSTEM
SYSTEME DE TRAITEMENT DE DONNEES
Patent Applicant/Assignee:
INTEL CORP,
Inventor(s):

COLLEY S,
RATTNER J,
COX G,
SWANSON R,
Patent and Priority Information (Country, Number, Date):
Patent: WO 8102477 A1 19810903
Application: WO 80US205 19800228 (PCT/WO US8000205)
Priority Application: WO 80US205 19800228
Designated States: DE GB JP AT CH DE FR GB LU NL SE
Main International Patent Class: **G06F-003/00**
International Patent Class: **G06F-07:00 ; G06F-09:00 ; G06F-13:00 ; G06F-15:16 ; G06F-15:20**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 139912

English Abstract
A data processor architecture wherein the processors recognize two basic types of objects, an object being a representation of related information maintained in a contiguously addressed set of memory locations. The first type of object contains ordinary data, such as characters, integers, reals, etc. The second type of object contains a list of access descriptors. Each access descriptor provides information for locating and defining the extent of access to an object associated with that access descriptor. The processors recognize complex objects that are combinations of objects of the basic types. One such complex object (94) defines an environment (18 or 20) for execution of objects (92, 93, 98, 106, 122) accessible to a given instance of a procedural operation. The dispatching of tasks to the processor is accomplished by hardware-controlled queuing mechanisms (36), dispatching-port objects (146) which allow multiple sets of processors (38) and (40) to serve multiple, but independent sets of tasks (14, 16). Communication between asychronous tasks or processes is accomplished by related hardware controlled queuing mechanisms (34) (buffered-port objects) (144) which allow messages to move between internal processes or input/output processes without the need for interrupts. A mechanism (42) is provided which allows the processors to communicate with each other. This mechanism is used to reawaken an idle processor to alert the processor to the fact that a ready-to-run process at a dispatching port needs execution.

French Abstract
Structure de processeur de donnees dans laquelle les processeurs reconnaissent deux types fondamentaux d'objets, un objet etant constitue par une representation d'informations connexes maintenues dans un groupe d'emplacements de memoire adresse en contiguite. Le premier type d'objets contient des donnees ordinaires, telles que des caracteres, des nombres entiers, reels, etc. Le deuxieme type d'objets contient une liste de descripteurs d'acces. Chaque descripteur d'acces fournit une information servant a localiser et definir l'etendue de l'acces a un objet associe a ce descripteur. Les processeurs reconnaissent des objets complexes constitues par des combinaisons d'objets des types fondamentaux. Un tel objet complexe (94) definit un environnement (18) ou (20) pour l'execution d'objets (92, 93, 98, 106, 122) accessible a un moment donne d'une operation de traitement. La repartition des taches aux processeurs est executee par des mecanismes (36) de mise en file d'attente commandes par le materiel, des objets (146) de points de connexion de repartition permettant a des groupes multiples de processeurs (38 et 40) d'executer des ensembles de taches (14, 16) multiples mais independantes. La communication entre des taches ou traitement asynchrones est executee par les mecanismes (34) relatifs de mise en file d'attente commandes par le materiel (objets de points de connexion dotes d'un tampon) (144) permettant la circulation des messages entre les traitements internes ou les operations d'entree/sortie sans que des interruptions soient necessaires. Un mecanisme (42) est prevu permettant la communication entre les processeurs. Ce mecanisme est utilise pour reactiver un

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Set     Items   Descripti
S1          5   TEFP? OR TEFPFEC OR EXTEND?()FAST()PATH?
S2      74517   PERSISTENT? OR RESIDENT? OR "IN"()(MEMOR? OR SRAM OR RAM) -
             OR TSR
S3       1151   S2(3N)(TABLE? OR GRAPH? OR CHART? OR TUPL? OR MATRIX? OR M-
             ATRICE?)
S4    3245513   SYNTAX? OR FORMAT? OR LANGUAGE? OR SCHEMA? OR SYSTEM?
S5       9280   (ACCESS? OR AVAILAB?)(4N)(LIMIT? OR PARAMET? OR OPEN OR CL-
             OSED OR PARTIAL? OR TIER? OR HIERARCH?)
S6        629   S3 AND S4
S7       8486   (DROP? OR END? OR KILL? OR STOP?)(3N)(COMMAND? OR SHUTDOWN?
              OR POWERDOWN OR (POWER OR SHUT)()(DOWN OR OFF))
S8          3   S6 AND S5
S9          3   S5 AND S6
S10        93   S3(10N)S4
S11        96   S8 OR S9 OR S10
S12        12   S11 AND IC=(G06F-007? OR G06F-017?)
S13        15   S8 OR S9 OR S12
S14         0   EXTEND?()FAST?()PATH?
S15        15   IDPAT S13 (sorted in duplicate/non-duplicate order)
S16        15   IDPAT S13 (primary/non-duplicate records only)
File 347:JAPIO Oct 1976-2002/May(Updated 020903)
         (c) 2002 JPO & JAPIO
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200261
         (c) 2002  Thomson Derwent
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16/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014044509 **Image available**
WPI Acc No: 2001-528722/200158
XRPX Acc No: N01-392356
Timing model generation method for electronic design automation system , **involves replacing memory** resident **lookup** table **with polynomial form when computed Chi-square result is greater than threshold**
Patent Assignee: SYNOPSYS INC (SYNO-N)
Inventor: CHANG S; WANG F
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6272664	B1	20010807	US 9890298	A	19980603	200158	B

Priority Applications (No Type Date): US 9890298 A 19980603
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6272664	B1		40	G06F-017/50	

Abstract (Basic): US 6272664 B1
NOVELTY - Linear least square error curve fitting computation is carried out on data points of stored lookup table with respect to selected polynomial form for determining value for set of coefficients. When computed Chi-square result is greater than threshold, table is replaced with polynomial form otherwise process is continued by selecting another polynomial form from same set of scalable forms.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for computer system.
USE - For electronic design automation system used for designing integrated circuit device such as ASIC, microprocessors, microcontrollers for generating memory resident timing models.
ADVANTAGE - A set of scalable polynomials are effectively and efficiently used to represent the timing and power information. By reducing lookup table models into polynomial models, memory usage requirements is significantly reduced and computation speed is increased.
DESCRIPTION OF DRAWING(S) - The figure shows the flowchart for translating memory inefficient lookup table timing models into memory efficient polynomial models.
pp; 40 DwgNo 9/19
Title Terms: TIME; MODEL; GENERATE; METHOD; ELECTRONIC; DESIGN; AUTOMATIC; SYSTEM; REPLACE; MEMORY; RESIDENCE; TABLE; POLYNOMIAL; FORM; COMPUTATION; SQUARE; RESULT; GREATER; THRESHOLD
Derwent Class: T01
International Patent Class (Main): **G06F-017/50**
International Patent Class (Additional): **G06F-007/60** ; **G06F-017/10** ; G06F-101/00
File Segment: EPI

16/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013576240 **Image available**
WPI Acc No: 2001-060447/200107
XRPX Acc No: N01-045245
Object graph serializing method using object oriented JAVA platform, involves examining each statement in temporary serialized form to determine if each statement is redundant
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: MILNE P S
Number of Countries: 092 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week

WO 200055727	A2	200009[redacted]	WO 2000US7238	A	20000316	[redacted]0107	B
AU 200038989	A	20001004	AU 200038989	A	20000316	200107	
US 6301585	B1	20011009	US 99271049	A	19990317	200162	
EP 1166204	A2	20020102	EP 2000918122	A	20000316	200209	
			WO 2000US7238	A	20000316		

Priority Applications (No Type Date): US 99271049 A 19990317
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200055727	A2	E	22	G06F-009/44	
	Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW				
	Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW				
AU 200038989	A			G06F-009/44	Based on patent WO 200055727
US 6301585	B1			G06F-017/00	
EP 1166204	A2	E		G06F-009/44	Based on patent WO 200055727
	Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE				

Abstract (Basic): WO 200055727 A2
NOVELTY - An object graph is serialized to a temporary serialized form with instantiation and assignment statements. The instantiation statements are deserialized to create the object graph copy, and default values are assigned to the object graph's properties. The temporary serialized statements are examined for redundancy and a final serialized form is written without the redundant statements.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) object graph serializing program stored in memory medium;
(b) computer **system** for serializing an object **graph** into a **persistent** form
USE - For serializing object **graph** into **persistent** form using object oriented JAVA platforms and object oriented JAVA **language** for persistent storage of object oriented components.
ADVANTAGE - Storing space is reduced as the redundant statements are not stored for final serialization. Properties of classes are accessed through public APIs to avoid reliance on private implementations of classes, thereby serialized forms are still deserializable even when private implementations are different across different platforms or across the same platform over time. Incremental serialization also includes error recovery and mechanisms to handle several special cases.
DESCRIPTION OF DRAWING(S) - The figure shows flowchart illustrating an incremental serialization.
pp; 22 DwgNo 2/3
Title Terms: OBJECT; GRAPH; METHOD; OBJECT; ORIENT; PLATFORM; STATEMENT; TEMPORARY; FORM; DETERMINE; STATEMENT; REDUNDANT
Derwent Class: T01
International Patent Class (Main): G06F-009/44; **G06F-017/00**
File Segment: EPI

16/5/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013563061 **Image available**
WPI Acc No: 2001-047268/200106
XRPX Acc No: N01-036372
Graphics rendering method in computer graphics system, involves executing captured hardware instruction corresponding to called rendering function of desired image
Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000311240	A	20001107	JP 200088445	A	20000328	200106	B
CN 1270366	A	20001018	CN 2000104923	A	20000330	200107	
KR 2001006855	A	20010126	KR 200014747	A	20000323	200152	
TW 463104	A	20011111	TW 2000105241	A	20000322	200248	

Priority Applications (No Type Date): US 99283386 A 19990331
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000311240	A		11	G06T-001/00	
CN 1270366	A			G06K-009/20	
KR 2001006855	A			G06T-011/00	
TW 463104	A			G06F-017/00	

Abstract (Basic): JP 2000311240 A

NOVELTY - The basic rendering function of graphics, which defined desired image, is coded as application program, and stored in host. The start identifier of application program is called by graphics device driver (15), and corresponding hardware instruction for rendering function of graphics is captured in the memory, and it is executed from the memory when the demand is arised from the graphics subsystem (10).

USE - For rendering graphics in computer graphics system.

ADVANTAGE - Since the hardware instruction corresponding to basic rendering function of **graphics** is captured **in memory** , the **system** operation of host is minimized during demand of rendering of desired image.

DESCRIPTION OF DRAWING(S) - The figure shows the hardware component diagram of graphics rendering system.

Graphics subsystem (10)

Graphics device driver (15)

pp; 11 DwgNo 2/4

Title Terms: GRAPHIC; RENDER; METHOD; COMPUTER; GRAPHIC; SYSTEM; EXECUTE; CAPTURE; HARDWARE; INSTRUCTION; CORRESPOND; CALL; RENDER; FUNCTION; IMAGE
Derwent Class: T01
International Patent Class (Main): **G06F-017/00** ; G06K-009/20; G06T-001/00; G06T-011/00
International Patent Class (Additional): G06F-009/44; G06F-009/45; G06T-001/60
File Segment: EPI

16/5/4 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013476690 **Image available**
WPI Acc No: 2000-648633/200063
XRPX Acc No: N00-480860

Method of representing a graphic object in memory by partitioning the object surface into cells and storing information about each cell and its links to adjacent cells in memory

Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC INFORMATION TECHNOLO (MITQ)
Inventor: OOSTERBAAN C E; PFISTER H; VAN BAAR J
Number of Countries: 026 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1024436	A2	20000802	EP 99123305	A	19991122	200063	B
JP 2000222601	A	20000811	JP 99309505	A	19991029	200063	
JP 3285563	B2	20020527	JP 99309505	A	19991029	200241	

Priority Applications (No Type Date): US 99240279 A 19990129
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1024436	A2	E	53	G06F-017/20	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 2000222601	A		28	G06T-017/00	

JP 3285563 B2 26 G0[redacted]15/00 Previous Publ. patent [redacted]2000222601

Abstract (Basic): EP 1024436 A2

NOVELTY - The surface of a graphic object is partitioned into cells with a grid resolution related to the screen image plane resolution. Each cell is bounded by defined grid points (940) related to image plane resolution. A single zero dimension surface element point is stored in memory for each cell and attributes of part of the object in each cell are assigned to each surface element and linked to adjacent cells.

DETAILED DESCRIPTION - The attributes can include surface position, color and opacity and a normal to the surface of the cell and offsets to the surface elements in the adjacent cells. Attributes assigned to each surface element can also include a velocity and a mass of the portion of the object in the cell. Elastic and damping constants associated with the cell links can also be stored. An INDEPENDENT CLAIM is included for a **system** for generating a representation of a **graphic** object **in memory** .

USE - In graphics processing.

ADVANTAGE - Sampling according to the screen resolution makes it easier to deform or otherwise manipulate objects.

DESCRIPTION OF DRAWING(S) - The figure shows a flow diagram of a surfelization process using distance mapping.

pp; 53 DwgNo 9/29

Title Terms: METHOD; REPRESENT; GRAPHIC; OBJECT; MEMORY; PARTITION; OBJECT; SURFACE; CELL; STORAGE; INFORMATION; CELL; LINK; ADJACENT; CELL; MEMORY

Derwent Class: T01

International Patent Class (Main): **G06F-017/20** ; G06T-015/00; G06T-017/00

International Patent Class (Additional): G06T-017/40

File Segment: EPI

16/5/5 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013199552 **Image available**

WPI Acc No: 2000-371425/200032

XRPX Acc No: N00-278450

Computerized maintenance support system **of motor vehicle production line, searches** table in memory **to judge maintenance personnel corresponding to detected failure of computer and forwards maintenance notice to him**

Patent Assignee: YOKOGAWA DENKI KK (YOKG)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000122899	A	20000428	JP 98293383	A	19981015	200032	B

Priority Applications (No Type Date): JP 98293383 A 19981015

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000122899	A		6	G06F-011/30	

Abstract (Basic): JP 2000122899 A

NOVELTY - Memory (1) stores table relating to maintenance data of computer (C) with data maintenance personnel. When computer failure is detected, the table is searched and personnel corresponding to detected failure is found and maintenance notice is sent to that personnel.

USE - In motor vehicle production line.

ADVANTAGE - As repairing failure notice is sent to the person concerned, stoppage of production activity due to delayed maintenance is prevented.

DESCRIPTION OF DRAWING(S) - The figure shows block diagram of maintenance support system is shown.

Memory (1)

Computer (c)

pp; 6 DwgNo 1/5

Title Terms: MAINTAIN; S[redacted]ORT; SYSTEM; MOTOR; VEHICLE; P[redacted]UCE; LINE; SEARCH; TABLE; MEMORY; JUDGEMENT; MAINTAIN; PERSONNEL; CORRESPOND; DETECT ; FAIL; COMPUTER; FORWARD; MAINTAIN; NOTICE
Derwent Class: P56; T01; T05; X22
International Patent Class (Main): G06F-011/30
International Patent Class (Additional): B23Q-041/08; G05B-023/02; **G06F-017/60**
File Segment: EPI; EngPI

16/5/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013059357 **Image available**
WPI Acc No: 2000-231225/200020
XRAM Acc No: C00-070357
XRPX Acc No: N00-174417
Meals menu preparation system **for dietitians, includes standard menu** table **stored** in memory **and menu evaluation unit which evaluates computed menu table, based in number of calorie units of standard table**
Patent Assignee: TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000050815	A	20000222	JP 98225916	A	1998081	200020	B

Priority Applications (No Type Date): JP 98225916 A 19980810
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000050815	A		12	A23L-001/00	

Abstract (Basic): JP 2000050815 A
NOVELTY - Menu preparation system including a material master file (2) which stores applicable foodstuffs for every illness and their weights for unit calorie, is new.
DETAILED DESCRIPTION - A material master file (2) stores applicable foodstuffs for every illness and their weights for unit calorie. A standard menu preparation table (7) stores number of calories corresponding to weight of each foodstuff. A menu preparation unit (17) prepares menu table based on input values and a menu evaluation unit (23) evaluates computed menu table, based on number of calorie units of standard menu table.
USE - The system is used by dietitians in the preparation of menus and for serving patients.
ADVANTAGE - The number of calories corresponding to the selected foodstuff is automatically calculated and the menu preparation burden of dietitians is mitigated. A warning signal is included for alarming incorrect foodstuffs input and correction of the weight.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the menu preparation system.
Material master file (2)
Standard menu preparation table (7)
Menu preparation unit (17)
Menu evaluation unit (23)
pp; 12 DwgNo 1/17
Title Terms: MEAL; MENU; PREPARATION; SYSTEM; STANDARD; MENU; TABLE; STORAGE; MEMORY; MENU; EVALUATE; UNIT; EVALUATE; COMPUTATION; MENU; TABLE ; BASED; NUMBER; CALORIE; UNIT; STANDARD; TABLE
Derwent Class: D13; T01
International Patent Class (Main): A23L-001/00
International Patent Class (Additional): **G06F-017/00** ; **G06F-017/60** ; G06F-019/00
File Segment: CPI; EPI

16/5/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012598739 **Image available**
WPI Acc No: 1999-404845/199934
XRPX Acc No: N99-301786
Pre-formatted allographic Arabic text for hypertext markup language document
Patent Assignee: UNIV MARYLAND BALTIMORE (UYMA-N)
Inventor: HABASH N Y
Number of Countries: 082 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9928831	A1	19990610	WO 98US25201	A	19981203	199934	B
AU 9917036	A	19990616	AU 9917036	A	19981203	199945	

Priority Applications (No Type Date): US 9767442 P 19971203
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9928831	A1	E	26	G06F-017/00	

Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

AU 9917036	A		G06F-017/00	Based on patent WO 9928831

Abstract (Basic): WO 9928831 A1
NOVELTY - A document stored on a disc or **in memory** as characters in **graphemic format** is subjected to a conversion process of the graphemes by a series of conversion rules into allographs according to predetermined graphotactics. During accessing a document, a text rendering process is performed, wherein graphotactics are not used and only one-to-one mapping is performed using a font on the screen. Conversion occurs only once per document while rendering occurs during each access
DETAILED DESCRIPTION - An independent claim is included for a text display apparatus from a computer-readable medium
USE - Rendering Arabic text on the Internet or in hypertext markup language documents such as home pages and web sites
ADVANTAGE - Efficient with respect to memory space and rendering time by treating Arabic characters as text
DESCRIPTION OF DRAWING(S) - The drawing illustrates a text rendering process according to the present invention
pp; 26 DwgNo 2/6
Title Terms: PRE; ARABIC; TEXT; LANGUAGE; DOCUMENT
Derwent Class: T01
International Patent Class (Main): **G06F-017/00**
File Segment: EPI

16/5/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011843987 **Image available**
WPI Acc No: 1998-260897/199823
XRPX Acc No: N98-205724
Method for Korean language Hangeul to Hanja character conversion - involves selecting word conversion mode or character conversion mode and accordingly referring lookup table **in** memory **of data processing** system **to perform conversion**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: LIM C S; RHO K Y; WU V
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5742838	A	19980421	US 93136431	A	19931013	199823	B

Priority Applications (No Type Date): US 93136431 A 19931015
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 5742838 A 19 G06F-017/21

Abstract (Basic): US 5742838 A

The method involves using a data processing system for selected Hangeul to Hanja character conversion in a structured document. The Hangeul characters from the document are stored in memory. When a character is input through the keyboard, a word or character conversion mode is selected. If character conversion mode is selected, each consecutive input Hangeul character is analyzed. The corresponding Hanja character is referred in a lookup table in the memory by the CPU. The Hanja character is then displayed on the display unit.

In the word conversion mode, the CPU locates two delimiters in the input Hangeul characters. The Hangeul characters between the delimiters are converted to corresponding Hanja characters by referring to the lookup table. When Hangeul characters are input through the keyboard a Hangeul text node structure is assembled. The structure includes a Hangeul character string and control information. The Hangeul string is accessed from the structure and subjected to conversion into corresponding Hanja phrases.

ADVANTAGE - Provides flexible and accurate conversion operation. Enables conversion of single or multiple Hangeul characters into corresponding Hanja characters.

Dwg.9b/9

Title Terms: METHOD; KOREAN; LANGUAGE; CHARACTER; CONVERT; SELECT; WORD; CONVERT; MODE; CHARACTER; CONVERT; MODE; ACCORD; REFER; TABLE; MEMORY; DATA; PROCESS; SYSTEM; PERFORMANCE; CONVERT
Derwent Class: T01
International Patent Class (Main): **G06F-017/21**
File Segment: EPI

16/5/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011145753 **Image available**
WPI Acc No: 1997-123677/199712
XRPX Acc No: N97-101964

Production management appts for e.g. engineering construction work analysis for insurance claim - updates production management table and displays name of person in charge, who is absent to office, in rectangular frame

Patent Assignee: TAISEI CONSTR CO LTD (TAKJ)
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
JP 9006842 A 19970110 JP 95147569 A 19950614 199712 B

Priority Applications (No Type Date): JP 95147569 A 19950614
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
JP 9006842 A 8 G06F-017/60

Abstract (Basic): JP 9006842 A

The appts has a management table with predefined **format** stored **in memory** . This **table** contains the recognition hole of the person in charge on any given day as well as his occupational description. The person in charge is determined based on the contents of the table and other information. Before starting the work, the data pertaining to the name of the person in charge is supplied through an input unit (6). A management table is generated and stored in the memory.

This table is displayed on a monitor (8) or it is output through a printer (9). The recognition code of person notified by the attendance management unit is compared with the contents of the management table.

The absence of the person in charge is obtained as a comparison result. In this case, the management table is updated and the name of the person who is absent is displayed in a box in the monitor. The name of the alternative candidate who is in charge is also printed on paper.

ADVANTAGE - Arranges responsible person to take charge. Generates hard copy print-out indicating name of person in charge. Discriminates responsible person who was absent to office.

Dwg.1/6

Title Terms: PRODUCE; MANAGEMENT; APPARATUS; ENGINEERING; CONSTRUCTION; WORK; ANALYSE; INSURANCE; CLAIM; UPDATE; PRODUCE; MANAGEMENT; TABLE; DISPLAY; NAME; PERSON; CHARGE; ABSENCE; OFFICE; RECTANGLE; FRAME
Derwent Class: T01; T05
International Patent Class (Main): **G06F-017/60**
International Patent Class (Additional): G07C-001/00
File Segment: EPI

16/5/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011010961 **Image available**
WPI Acc No: 1996-507911/199651
XRPX Acc No: N96-427947

Computerised FEM simulation for acoustic behaviour of body surrounded by fluid - involves computing element matrix coefficients from fluid medium elements and solving equation providing acoustic field variable for mesh

Patent Assignee: AT & T IPM CORP (AMTT); AT & T CORP (AMTT); LUCENT TECHNOLOGIES INC (LUCE)
Inventor: BURNETT D S; HOLFORD R L; LOVELL H R; STORER B D
Number of Countries: 008 Number of Patents: 011
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 743610	A1	19961120	EP 96303209	A	19960508	199651	B
FR 2734379	A1	19961122	FR 9511377	A	19950928	199703	
AU 9652260	A	19961128	AU 9652260	A	19960513	199704	
CA 2174889	A	19961119	CA 2174889	A	19960424	199712	
US 5604893	A	19970218	US 95443534	A	19950518	199713	
BE 1009459	A3	19970401	BE 951079	A	19951228	199719	
NZ 286567	A	19970624	NZ 286567	A	19960513	199732	
AU 701884	B	19990211	AU 9652260	A	19960513	199918	
CA 2174889	C	20000111	CA 2174889	A	19960424	200023	
EP 743610	B1	20000412	EP 96303209	A	19960508	200023	
DE 69607678	E	20000518	DE 607678	A	19960508	200031	
			EP 96303209	A	19960508		

Priority Applications (No Type Date): US 95443534 A 19950518
Cited Patents: 1.Jnl.Ref
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 743610	A1	E	48	G06F-017/50	
Designated States (Regional): DE GB					
FR 2734379	A1			G06F-017/11	
AU 9652260	A			G06F-017/13	
CA 2174889	A			G06F-019/00	
US 5604893	A		25	G06F-017/16	
BE 1009459	A3		72	G06F-000/00	
NZ 286567	A			G06F-017/50	
AU 701884	B			G06F-017/13	Previous Publ. patent AU 9652260
CA 2174889	C	E		G06F-019/00	
EP 743610	B1	E		G06F-017/50	
Designated States (Regional): DE GB					
DE 69607678	E			G06F-017/50	Based on patent EP 743610

Abstract (Basic): EP 743610 A

The FEM simulation method involves subdividing at least the fluid medium into a pattern of elements referred to as a mesh for storage in memory. For each mesh element a set of element matrix coefficients is computed in the memory. All the element matrix coefficients are

assembled into a **system matrix** and stored **in memory**. The **system matrix** equation is solved in the data processing element to create a description of the values assumed by an acoustic field variable throughout the mesh. The description is then recorded in data storage.

The subdivision step involves construction an inner boundary of the fluid medium coinciding with the outer surface of the body. An oblate bounding spheroid is constructed enclosing the inner fluid boundary. A space bounding the spheroid is filled with infinite elements where each infinite element is bounded by a base, at least three side faces and an outer face. Each respective base lies on the bounding spheroid. Each respective outer face belongs to an oblate spheroidal surface confocal with the bounding spheroid. Each respective side face is a locus of hyperbolas confocal with the bounding spheroid. The outer face recedes to an infinite oblate radius.

ADVANTAGE - Provides greatly improved efficiency in acoustic modelling of elongate structures.

Dwg.1/12

Title Terms: COMPUTER; SIMULATE; ACOUSTIC; BEHAVE; BODY; SURROUND; FLUID; COMPUTATION; ELEMENT; MATRIX; COEFFICIENT; FLUID; MEDIUM; ELEMENT; SOLVING; EQUATE; ACOUSTIC; FIELD; VARIABLE; MESH

Derwent Class: T01

International Patent Class (Main): G06F-000/00; **G06F-017/11** ; **G06F-017/13** ; **G06F-017/16** ; **G06F-017/50** ; G06F-019/00

International Patent Class (Additional): **G06F-017/10**

File Segment: EPI

16/5/11 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX

010705725 **Image available**

WPI Acc No: 1996-202680/199621

Related WPI Acc No: 1999-613181

XRPX Acc No: N96-170072

Charge unit price determination and information apparatus for communications system **- analyses called party number to determine calling and receiving locations which are used as** parameters **to** access **a table of unit charges**

Patent Assignee: KOKUSAI DENSHIN DENWA CO LTD (KOKU)

Inventor: TAKEUCHI Y; WATANABE F

Number of Countries: 003 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2294611	A	19960501	GB 9521882	A	19951025	199621	B
JP 8125783	A	19960517	JP 94260178	A	19941025	199630	
JP 8242316	A	19960917	JP 9541735	A	19950301	199647	
GB 2294611	B	19991103	GB 9521882	A	19951025	199948	
US 5978456	A	19991102	US 95541119	A	19951011	199953	

Priority Applications (No Type Date): JP 9541735 A 19950301; JP 94260178 A 19941025

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2294611	A		142	H04Q-007/22	
JP 8125783	A		24	H04M-015/00	
JP 8242316	A		18	H04M-015/00	
GB 2294611	B			H04Q-007/22	
US 5978456	A			H04M-015/00	

Abstract (Basic): GB 2294611 A

The charge unit price determination/information apparatus includes a processor (2) to analyse a called party number and specify a receiving destination. A price determination processor (3) specifies a communication path from the calling location to the receiving location and calculates the unit price. An information unit (8) provides the unit price information to the calling terminal.

In addition, the unit price information can be provided to the receiving terminal well as the calling terminal. Pref. the price determination processor accesses a charge unit price **table** stored **in memory** (4) using the calling and receiving locations as parameters.

USE - For providing portable telephone users with charge unit price information when charging according to location and therefore when caller may not know unit price. Also for informing collect call recipients of unit price of incoming call.

Dwg.1/36

Title Terms: CHARGE; UNIT; PRICE; DETERMINE; INFORMATION; APPARATUS; COMMUNICATE; **SYSTEM** ; ANALYSE; CALL; PARTY; NUMBER; DETERMINE; CALL; RECEIVE; LOCATE; PARAMETER; ACCESS; TABLE; UNIT; CHARGE
Index Terms/Additional Words: TELEPHONE; NETWORK; PORTABLE; COLLECT
Derwent Class: W01; W02
International Patent Class (Main): H04M-015/00; H04Q-007/22
International Patent Class (Additional): H04M-003/42; H04M-015/08
File Segment: EPI

16/5/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010166619 **Image available**
WPI Acc No: 1995-067872/199510
XRPX Acc No: N95-053880
Multiple natural languages data processing system with user-dialogue - has connection table in memory **that links user-program and information for access in different** languages
Patent Assignee: COMPUTERVISION CORP (COMP-N)
Inventor: CHARLES J; MERZ L
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4325096	A1	19950202	DE 4325096	A	19930727	199510	B
DE 4325096	C2	19981217	DE 4325096	A	19930727	199903	

Priority Applications (No Type Date): DE 4325096 A 19930727
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4325096	A1		47	G06F-003/16	
DE 4325096	C2			G06F-017/28	

Abstract (Basic): DE 4325096 A

The data processing system has a central computer (40) to which are linked multiple user stations (42) via communication links (44). The user stations have keyboard and monitor (48) facilities, and provide access to dedicated and general areas of memory.

The system allows a natural language, e.g. English, German, etc. to be selected and information to be accessed in that **language** . A connection **table in memory** links the user program and the information in such a way that a word search procedure identifies the correct language.

ADVANTAGE - Allows use of data processing system in multiple natural language.

Dwg.1/33

Title Terms: MULTIPLE; NATURAL; LANGUAGE; DATA; PROCESS; SYSTEM; USER; DIALOGUE; CONNECT; TABLE; MEMORY; LINK; USER; PROGRAM; INFORMATION; ACCESS; LANGUAGE
Derwent Class: P86; T01; W04
International Patent Class (Main): G06F-003/16; **G06F-017/28**
International Patent Class (Additional): G10L-003/00
File Segment: EPI; EngPI

16/5/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008823283 **Image available**
WPI Acc No: 1991-327296/199145
XRPX Acc No: N91-250699

Database transactions for data processing system - supports sequential batch applications which permits continued enumeration of sequence of objects across transaction commit

Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: COYLE D J; LINDSAY B G
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 455440	A	19911106	EP 91303833	A	19910426	199145	B
US 5220665	A	19930615	US 90516363	A	19900430	199325	
EP 455440	A3	19930915	EP 91303833	A	19910426	199509	
EP 455440	B1	19950906	EP 91303833	A	19910426	199540	
DE 69112694	E	19951012	DE 612694	A	19910426	199546	
			EP 91303833	A	19910426		

Priority Applications (No Type Date): US 90516363 A 19900430
Cited Patents: NoSR.Pub; 1.Jnl.Ref
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 455440	A				
Designated States (Regional): DE FR GB					
US 5220665	A		13	G06F-007/00	
EP 455440	B1	E	16	G06F-011/14	
Designated States (Regional): DE FR GB					
DE 69112694	E			G06F-011/14	Based on patent EP 455440

Abstract (Basic): EP 455440 A

The data processing system supports batch processing of an application-specified sequence of objects in databases while permitting the continued enumeration of such sequence of objects following a transaction commit. A number of queries are defined. Each query specifies sets of objects within the data processing system associating a named cursor with each query. Each named cursor includes one scan which may be utilised to evaluate and enumerate an associated query.

At least one named cursor is designated as a persistent cursor. The status of each persistent cursor is stored in a table along with the state of any included scan, and a query evaluation state in response to a transaction commit. A selected position within the query may be reestablished utilising the persistent cursor table following the transaction commit.

ADVANTAGE - Permits efficient processing of batch operations without unduly interfering with on-line transactions. (15pp Dwg.No.2/10)

Title Terms: DATABASE; TRANSACTION; DATA; PROCESS; SYSTEM; SUPPORT; SEQUENCE; BATCH; APPLY; PERMIT; CONTINUE; SEQUENCE; OBJECT; TRANSACTION; COMMIT
Derwent Class: T01
International Patent Class (Main): **G06F-007/00** ; G06F-011/14
International Patent Class (Additional): G06F-015/40; G06F-015/403; **G06F-017/30**
File Segment: EPI

16/5/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008180406 **Image available**
WPI Acc No: 1990-067407/199010
XRPX Acc No: N91-039848

Managing host to work-station file transfer - transfers multiple files by constructing appropriate data structures and file names for each file

Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: PETERS A M; SEHORNE M A

Number of Countries: 006 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
BR 8902762	A	19900201				199010	B
EP 413074	A	19910220	EP 89480128	A	19890816	199108	N
US 4999766	A	19910312	US 88205969	A	19880613	199113	
EP 413074	B1	19960327	EP 89480128	A	19890816	199617	
DE 68926114	E	19960502	DE 626114	A	19890816	199623	N
			EP 89480128	A	19890816		

Priority Applications (No Type Date): US 88205969 A 19880613; EP 89480128 A 19890816; DE 626114 A 19890816

Cited Patents: 3.Jnl.Ref

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 413074	A				
Designated States (Regional): DE FR GB IT					
EP 413074	B1	E	24	G06F-015/16	
Designated States (Regional): DE FR GB IT					
DE 68926114	E			G06F-015/16	Based on patent EP 413074

Abstract (Basic): EP 413074 A

The data processing **system** comprises a memory, a data storage device and running under one of a number of operating **systems** , and a work station. The work station has a memory, a display, a keyboard including a number of function keys and a data storage device with a **resident** profile **table** comprising appropriate data structures and names for mapping a file on the work station to a file on the host computer depending on the operating **system** under which the host computer is running.

A method of transferring the file from the data storage device of the work station to the data storage device of the host computer comprises the steps of: accessing the profile table to determine an appropriate data structure and file name for the file when transferred to the data storage device of the host computer. The appropriate data structure and file name for the file is constructed. The file, is transferred with the appropriate data structure and file name from the data storage device of the work station to the data storage device on the host computer.

ADVANTAGE - Maintains consistant filename conventions between files exending on multiple host and work stations. (First major country equivalent to BR8902762)

Dwg.1/9

BR 8902762 A

The data processing **system** comprises a memory, a data storage device and running under one of a number of operating **systems** , and a workstation.

The workstation has a memory, a display, a keyboard including a number of function keys and a data storage device with a **resident** profile **table** comprising appropriate data structures and names for mapping a file on the workstation to a file on the host computer depending on the operating **system** under which the host computer is running. A method of transferring the file from the data storage device of the workstation to the data storage device of the host computer comprises the steps of: accessing the profile table to determine an appropriate data structure and file name for the file when transferred to the data storage device of the host computer.

The appropriate data structure and file name for the file is constructed.

The file, is transferred with the appropriate data structure and file name from the data storage device of the workstation to the data storage device on the host computer. ADVANTAGE - Maintains consistant filename conventions between files exending on multiple host and workstations.

(First major country equivalent to BR8902762) (23pp Dwg.No.1/9

Title Terms: MANAGE; HOST; WORK; STATION; FILE; TRANSFER; TRANSFER; MULTIPLE; FILE; CONSTRUCTION; APPROPRIATE; DATA; STRUCTURE; FILE; NAME; FILE

Derwent Class: T01
International Patent Class (Main): G06F-015/16
International Patent Class (Additional): G06F-013/14
File Segment: EPI

16/5/15 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007117691
WPI Acc No: 1987-117688/198717
XRPX Acc No: N87-088194
Phase rotation method of digital signal - applying partial address signal for look-up table in memory **together with rotation control signals as additional address signals**
Patent Assignee: NORTHERN TELECOM LTD (NELE); STC PLC (STTE)
Inventor: FEARNHEAD G R; FURNACE M L C; GALE S J; FEARNHEAD G; FURNACE M; GALE S
Number of Countries: 008 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 220005	A	19870429	EP 86307657	A	19861003	198717	B
GB 2181907	A	19870429	GB 8525702	A	19851018	198717	
US 4796188	A	19890103	US 86915394	A	19861006	198904	
GB 2181907	B	19891011				198941	
CA 1261949	A	19890926				198945	
EP 220005	B1	19931201	EP 86307657	A	19861003	199348	
DE 3689353	G	19940113	DE 3689353	A	19861003	199403	
			EP 86307657	A	19861003		

Priority Applications (No Type Date): GB 8525702 A 19851018
Cited Patents: 1.Jnl.Ref; A3...9017; GB 2153177; No-SR.Pub; WO 8202637
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 220005	A	E	7		
Designated States (Regional): DE FR IT NL SE					
US 4796188	A		6		
EP 220005	B1	E	11	G06F-001/02	
Designated States (Regional): DE FR IT NL SE					
DE 3689353	G			G06F-001/02	Based on patent EP 220005

Abstract (Basic): EP 220005 A
The method uses a memory having a look-up table (12) to which are applied, as partial address signals, an input digital signal, whose phase is to be rotated, and, as additional address signals, rotation control signals. The phase rotated signal is obtained from the output of the memory, and the phase is to be rotated in a range up to 360 degrees.
The range is divided into four 90 degree quadrants and the look-up table is provided for only one of these quadrants. It is then determined which quadrant the input signal is in and the input signal is transformed, if necessary, to provide a suitable partial address signal for the look-up table.
ADVANTAGE - Reduces size of PROM required for look-up table.
3/6
Title Terms: PHASE; ROTATING; METHOD; DIGITAL; SIGNAL; APPLY; ADDRESS; SIGNAL; UP; TABLE; MEMORY; ROTATING; CONTROL; SIGNAL; ADD; ADDRESS; SIGNAL
Derwent Class: T01; W06
International Patent Class (Main): G06F-001/02
International Patent Class (Additional): G01S-005/14; G06F-012/06; H03H-017/08; H04L-

because joining the temporary tables in main memory and the tables in the database system is a very expensive operation in a loosely-coupled system. A loosely-coupled system is defined as one in which the inference engine and the database system are two separate systems that communicate with each other. On the other hand, we define a system that integrates inference capability and data retrieval/manipulation capability as a tightly-coupled system. Even in a tightly-coupled system, temporary tables must be created only when it is beneficial to improving the performance. However, this decision has to be made by the query optimizer, rather than dictated by the structure of the query representation. In Ullman's method, the temporary tables are created and the query processed according to the data structure representing the query. This data structure, in turn, is imposed by the structure of the rules that the users write in the system before issuing the query. In the following, the representation of logic queries is transformed into a normal form representation (EDNF). The algorithm to process the query based on the EDNF, as well as the algorithm to obtain the EDNF given a query, is subsequently described. First, the data structure program graph will be defined. The program graph is the representation of the query that reflects the structure implied in the rules. For example, consider the following rules: r1: a(X,Y) < - g(X,Z) & c(Z,Y) r2: g(X,Z) < - d(X,W) & e(W,Z) where < - is the implication operator. Suppose the query ?a(X,5) is asked. Then the corresponding program graph is as shown in Fig. 1. In Fig. 1, "b" and "f" indicate that the corresponding argument of a goal or a variable of a rule is bound or free, respectively. In Fig. 1, a(), g(), d(), e(), and c() are goals, and r1() and r2() are rules. In a rule, all the variables included in the rule are enumerated; therefore, r1 has variables X, Y, and Z, while r2 has X,Z, and W. In constructing the program graph, binding information on variables and arguments are propagated down by means of unification. Now a program graph for a recursive query is constructed. Consider the following rules: r1: a(X,Y) < - e(X,Y) r2: a(V,W) < - e(V,Z) & a(Z,W) Suppose the question ?a(X,5) was asked. Then, the program graph is as shown in Fig. 2. In Fig. 2, we have an arc from r2 to a because the goal a(f/*,b(5)/*) appears repetitively with the same binding information. Since we cannot unify the variables in an existing node, we use mapping of variable names; in this case, it indicates X in goal a is mapped to Z in rule r2. In general, mapping is necessary whenever an existing node is encountered while constructing the program tree. Notice the mapping does not necessarily indicate presence of recursion (directed cycle), because mapping is also needed when an undirected cycle is formed. In the straightforward evaluation algorithm, we have to create a temporary table for each node in the program graph, and the query is processed by evaluating each node according to the partial order dictated by the program graph. If there is a cycle, the nodes in the cycle must be evaluated repetitively until a fixpoint is reached. Evaluation of a rule node is done by joining the evaluations of the goals below, and that of a goal node is done by unioning the evaluations of the rules below. The idea of the present technique is to eliminate unnecessary temporary tables and to eliminate predefined execution structure (i.e., the partial order dictated by the program graph). For example, in Fig. 1, the straightforward algorithm requires four temporary tables, and in Fig. 2, three temporary tables. For more complex queries, the number of temporary tables increases. In contrast, the present technique would require only ONE temporary table in either case. It also allows processing the goals in an arbitrary order, i.e., there is no partial order dictated by the program graph. This is an essential feature for effective optimization of query execution. The EDNF of a program graph is a set of two-level trees, in which the root is the queried goal (Query Goal) and a leaf is a leaf in the program graph. Further, a tree can contain a cycle indicating recursion, in which the root also appears as a leaf. We call such a tree a cyclic tree. Algorithm EDNF produces the EDNF of a program graph according to the notation defined in Fig. 5. To describe the algorithm, we use the following notation: Edgemap: Mapping function described on an edge. The function maps the variable name on the head side of the edge to the variable name on the tail side of the edge. Accmapping: Accumulative mapping function that maps a variable name to another variable name for a unique path between a node and the node where this mapping chain begins. Accmapping is obtained as a composition of Edgemaps along this path. - For example, if variable X in Node 1 was mapped to Y in Node 2, the variable Y in Node 2 to Y in Node 3, and the variable Y in Node 3 to Z in Node 4, then Accmapping(X) = Z at Node 4. Forest: EDNF of a program graph. - Querygoal: The goal asked as a query. This becomes the root of the program graph. Node: A node in the program graph. Algorithm EDNF(Node,Forest,Edgemap,Accmapping,Querygoal) For every variable (X) in Node newmapping(X):=Edgemap(Accmapping) If Node is a goal node Then If Node is a leaf Then Replace__variable__names Forest:=Construct__tree(Node) Else if Node is Querygoal and this is not the first visit to Querygoal Then Replace__variable__names Tree:= Construct__tree(Node) Tag the tree as a cyclic tree Forest: =Tree Else /*nonleaf node or Querygoal at the first visit*/ Forest:=theyÙ

For each child (C) of Node and the corresponding edge (E) EDNF(C,Subforest, EdgemapE, newmapping, Querygoal) Forest:= Forest U Subforest Else If Node is a rule node then Forest:=theyÙ For each child (C) and the corresponding edge (E) EDNF(C,Subforest, EdgemapE, newmapping,Querygoal) Forest:=XPROD(Forest,Subforest) END Replace__variable__names:For every variable (X) in the Node, replace X with newmapping -1(X).

Disclosure Text (2):
Construct__tree(Node): Construct the tree having Node as a sole leaf and Querygoal as the root. XPROD(Forest1, Forest2): Construct a set of trees, each tree t being constructed as follows: For each t1 e Forest 1 and t2 e Forest2, Leaves(t):=Leaves(t1)U Leaves(t2) Root(t):=Root(t1):=Root(t2) In addition, if either t1 or t2 (or both) is tagged as a cyclic tree, then t is also tagged as a cyclic tree. - Note that we used set union on Leaves because join between two identical nodes with the same binding results in the same node.
EDNF(Querygoal,Forest,Indentity__mapping, Identity__mapping, Querygoal) will produce the desired EDNF and return the result in the variable Forest. Algorithm for processing logic queries based on EDNF Notation: NCT: set of noncyclic trees in the EDNF CT: set of cyclic trees in the EDNF Algorithm Process__Query(EDNFquery,Result) 1) Result:=theyÙ 2) For each tree t e NCT Result:=Result U Eval(t) 3) Repeat until no change in Result For each tree t' e CT Result:=Result U Eval(t') END Eval(t): Join all leaf nodes in this tree and project the variables in the root Step 3 of Algorithm Process__Query can be performed in various alternative ways. For example, the following process will achieve the same result. Repeat until no change in Result For each tree t' e CT Result:=Result U Obtain__fixpoint(t') where Obtain__fixpoint(t'): Repeat until no change in Result Result:=Result U Eval(t')
Reference J. Ullman, "Implementation of Logical Query Languages for Databases," ACM Trans . on Database Systems (1985).

☐ 5. Document ID: NN84056391

L5: Entry 5 of 6 File: TDBD May 1, 1984

TDB-ACC-NO: NN84056391

DISCLOSURE TITLE: Formatter for Formula Output

L5: Entry 5 of 6 File: TDBD May 1, 1984

DOCUMENT-IDENTIFIER: NN84056391
TITLE: Formatter for Formula Output

Disclosure Text (1):
- The design of a formatter for use in a word processing system which can transform a natural language input into conventionally printed single or multiline formulas is described. The natural language input is described in the preceding article. The following assumptions apply to the formatter herein described: 1. The input data conforms to the formula method shown in the preceding article. 2. Parsing into elements of the formula is done as described in the preceding article. 3. A memory matrix is used which has a character position for each character on a row, and a row of characters at each half-index position (i.e., for each half line). On output, subscripted and superscripted characters may be employed. 4. At the completion of

the formatting process, this memory matrix will be outputted in a manner appropriate to a particular output device. The basic approach is to format the line left to right, an element at a time. Whenever an element causes a shift in the base line of the formula, then the formatter shifts the previously completed elements down in memory. The base line is the line on which are located the element delimiters, such as the equal sign and the arithmetic operators between elements. This is not easily described by means of an example. See Fig. 1. The input expression is: F = INT (A,B) (1+2x OVER (3Z+C)) dx This is parsed into two elements, separated by the equal sign. The initial base line is on the second line of the memory matrix. The figures depict the memory matrix of half-line intervals; the characters will be printed or displayed with half-indexing as required. The integration indices a and b are placed in the subscript and superscript positions. Normal processing continues until the numerator term of an "OVER" control is reached. The formatter scans ahead after each potential delimiter to see if another control must be processed. When the "OVER" control is found, then the numerator and denominator are delimited as previously described. The base line is shifted down one half line, which means shifting all previous elements and delimiters down. The shorter of the two terms (the numerator, in this example) is centered over the denominator and underscores are entered. Processing to the end of the expression continues on the new base line. Note that the underscores under the term "2x" will print so that they form a line beside the "+" sign. To further illustrate the method, consider the variation on this case, as shown in Fig. 2. The input is: F = INT(A,B) (1 + 2X OVER (3Z+C)) OVER (4 X2) dx The first step is identical to the example in Fig. 1. The second step begins the same, but another "OVER" control is found. The numerator for this second "OVER" is between the parentheses. In this case, the base line must shift down one full line because the numerator covers two lines itself. The formatter determines the extent of the numerator by scanning the previously processed data. The rule is that the base line must be moved to the next half-line position below the numerator. Note that, according to the rules of the formula method, the parentheses delimiting the numerator are dropped. Note, also, that the parentheses around the "4 X2" term are required so that the term "dx" appears on the base line. Fig. 3 is an example of a "MAT" input control with an "OVER" control. The input is: M = (MAT(a1 b1 c1, a2 b2 c2)) OVER 2 Calculating the dimensions of the matrix from the input is straightforward. When the "OVER" control is encountered, then the rule says the base line must go down to the next available half-line, and the parentheses are dropped. The formatter illustrated herein, taken together with the preceding article, allows a word processor to handle technical typing. The formatter uses an output memory matrix and a technique of progressively shifting the base line down, as required. The formatter can be made as complex as desired to handle other symbols or special notation requirements, and it may be designed to support either a printer or display.

☐ 6. Document ID: NA8106284

L5: Entry 6 of 6 File: TDBD Jun 1, 1981

TDB-ACC-NO: NA8106284

DISCLOSURE TITLE: On Board Logic for Multi Dot Thermal Printhead. June 1

L5: Entry 6 of 6 File: TDBD Jun 1, 1981

DOCUMENT-IDENTIFIER: NA8106284

dots (say, 2000), if they are addressed in subgroups similar to a memory scheme without some latching capability, the selection proceeds slowly from group to group at the heating rate of several milliseconds per group. With latching, the selection process can rapidly go from group to group with the heating delay being incurred once for the head as a whole. The embodiments shown are of the latter type, with a shift register providing a serial variable time multiplexed scheme for quick dot selection instead of a memory-type matrix selection scheme. This technique provides several dividends in simplifying interface electronics for the various applications, as illustrated in Figs. 3, 4 and 5. Since integrated electronics require high volume applications to amortize start-up costs, it is important to design as general a chip as possible. The variety of applications compatible with this interface insures that the high volume criterion is satisfied for this approach.

Terms	Documents
L4 and (syntax$ or language$ or syntact$ or schema$)	6

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☐ 1. Document ID: NN9510223

L7: Entry 1 of 19 File: TDBD Oct 1, 1995

TDB-ACC-NO: NN9510223

DISCLOSURE TITLE: Dynamic Port Allocation in a Multi-Process Transmission Control Protocol/ Internet Protocol Client/Server Application

L7: Entry 1 of 19 File: TDBD Oct 1, 1995

DOCUMENT-IDENTIFIER: NN9510223
TITLE: Dynamic Port Allocation in a Multi-Process Transmission Control Protocol/ Internet Protocol Client/Server Application

Disclosure Text (1):
Disclosed is a method, in a multi process client/server system, of implementing Transmission Control Protocol/Internet Protocol (TCP/IP) "Sockets" protocol as an alternative to Named Pipe protocol. - In a Named Pipes implementation of a client/server system, the server program maintains one end of a named pipe whose name is known to the client program. When the client program need to communicate with the server to read or write data, the client issues an OPEN command to the Named Pipe. On a successful Open, the client then issues READ and WRITE commands as required, and then issues a CLOSE command. Between the OPEN and CLOSE commands, the Named Pipe is not available to any other client. This scenario would be acceptable if only one client required access. Typically, a server needs to be able to service many clients concurrently. Named Pipe protocol allows multiple instances of a process to replicate the same pipe name. When a client issues an OPEN, the OS/2* File System identifies a free instance of the pipe and establishes the connection. This is transparent to the client. The TCP/IP sockets protocol, however, does not allow a socket number (equivalent to a Named Pipe "Name") to be replicated across multiple processes. Each instance must have a unique number. In implementing TCP/IP sockets as an alternative protocol (to enable remote clients), it is important that the communication protocol could be changed without extensive rewriting of the applica tion program. It is obviously not practicable to make each client aware of all of the multiple port numbers on the server. Therefore, the following process was devised: On the server, a parent program ("LAUNCH") manages the processes. The launch first creates a structure in Named Shared Memory as follows: typedef struct { PID ulPID; //Process ID USHORT usPort; //TCP/IP Port Number for this //Process USHORT fStatus; //Current Status of the Port double reserve_time; //Timestamp when the Port was //Reserved } PROCESS_DATA, *PPROCESS_DATA; Launch then starts one or more instances of the server process and stores the Process ID (PID) of the process just started in a row of the structure. As each instance of the server process initializes, it issues a TCP/IP command to initialize a socket. TCP/IP returns a unique port number. The server process stores this port number in its own slot (identified by PID) in the shared memory table, and sets its status to FREE. Launch then creates a TCP/IP socket with a predefined port number, which is known to the client processes (the "Public Port"). The client knows only the identity of this public port, and it is to this port that all OPEN requests are directed. An OPEN

request, whether in TCP/IP or Named Pipe protocol, results in a HANDLE being returned. This handle is then used by subsequent READ and WRITE calls, and is destroyed by the CLOSE.

Disclosure Text (2):
When the TCP/IP protocol code in the client receives an OPEN request, the following sequence of events takes place: The OPEN is directed to the TCP/IP Public Port on the server. A WRITE request is issued, with a data content of "REQUEST PORT". The server does a lookup on the table to find the first port with a status of FREE. It returns the port number to the client and marks the table entry as RESERVED. The client issues a CLOSE to the Public Port, and issues an OPEN to the Port Number it just received. The server receives the OPEN, marks the table entry as BUSY, and waits for READ and/or WRITE commands from the client. The client TCP/IP code returns the HANDLE to the application program, which then issues READ and/or WRITE commands followed by a CLOSE. On receiving the CLOSE, the server breaks the connec tion with the client and marks the table entry as FREE. Thus, in this process, the client issues an OPEN and receives a HANDLE. At the application program level, this part of the TCP/IP process appears identical to the Named Pipe protocol. The fact that a port other than the public port was dynamically allocated is transparent to the application, enabling it to operate under either communication protocol without changes at the application level. * Trademark of IBM Corp.

☐ 2. Document ID: NN9412443

L7: Entry 2 of 19 File: TDBD Dec 1, 1994

TDB-ACC-NO: NN9412443

DISCLOSURE TITLE: Memory Adapter Improvements for Personal Computers

L7: Entry 2 of 19 File: TDBD Dec 1, 1994

DOCUMENT-IDENTIFIER: NN9412443
TITLE: Memory Adapter Improvements for Personal Computers

Disclosure Text (1):
Described is an architectural implementation for a memory adapter that provides improvements in the areas of flexibility, capacity and compatibility for standard Personal Computers (PCs) and those equipped with a Micro Channel* (MC). The technique implements two distinct modes of operation; straddle mode and contiguous mode to provide improvements to existing memory adapters and is intended to be updatable for future memory technology. In prior art, the certain memory adapters fell into two categories, each of which had disadvantages. For example, 0-6 megabyte (MB) and 0-8 MB memory adapters were designed to be configured by means of a set configuration programs from reference diskettes, but were limited to capacities of 6 and 8 MBs, respectively. Recently enhanced memory adapters had a capacity of up to 32 MBs, but used a combination of a hard disk boot track initialization programs and Read Only Memory (ROM) programs to configure its memory. Follow-on memory adapters used only ROM programs, but had limited capacity. Typically, the prior art memory architecture was designed to allow the flexibility of using the same options across the entire product line. The PC memory was architected with three distinct interspersed address regions in which the system memory, such as memory into which

an operating system and application code may be placed. The three interspersed address regions involved non-system memory, such as a buffer memory belonging to graphics, or other types of adapters.

Disclosure Text (2):
System memory would exist at address ranges 0 to 640K-1, 1M going toward 16M-1, and 16M going toward 4G-1. Non-system memory would exist from 640K to 1M-1, from 16M-1 going backward toward 1M, and from 4G-1 going backward toward 16M. The 0 to 640K-1 to 1M-1 address ranges for system and non-system memory were considered fixed by the existing memory architecture. It was assumed that neither block of memory would expand outside either address range. The 1M to 16M-1 and 16M to 4G-1 address ranges worked differently. System memory was architected to start at the lower end of each of these address ranges and to go upward toward the high end, while non-system memory was architected downward, or backward, toward the low end of each of these address ranges. Non-system memory was intended to take precedence over system memory in each address range where they came into conflict for the same address space. The overall intent was that the hardware with the non-system memory would place that memory as high as possible in each of the two address ranges. Also, that the system would be configured starting at the 1M address and going contiguously until the first block of non-system memory was encountered, or until the end of available system memory had been reached, whichever came first. If non-system memory had been encountered and there remained more system memory to be configured, then the remainder was configured starting at address 16M and went contiguously until the first block of non-system memory in the other range was reached, or until the end of available system memory had been reached, whichever came first. If non-system memory had been reached and there was more system memory to be configured, then this remainder memory was disabled and not used. There were practical reasons why system and non-system memory were not simply configured into two large contiguous blocks. Various situations and compatibility issues resulted in there being three separate blocks of each type of memory. The reason a block of non-system memory was architected to exist in the 640K to 1M-1 address range was due to the need to maintain compatibility with the original microprocessor and the address space limiting their addressing capability to 1 MB. The separation of the remainder of the address space in 32-bit PCs into 1M to 16M-1 to 4G-1 address ranges was a more recent addition. The non-system memory space of 640K to 1M-1 was becoming crowded and this was added to allow adapters with non-system memory to put that memory at higher addresses in PCs with either 24-bit or 32-bit addressing capability. PCs equipped with different microprocessors had only 24-bit addressing capability which limited them to addressing only up to 16MBs. Since it was desirable that adapters with non-system memory be able to operate PC with different types of microprocessors with their non-system memory being put at identical addresses, it was decided that a block of non-system memory should be defined within the first 16MBs of address space in PCs with 32-bit addressing. Prior to the definition of an additional block of non-system memory within the 1M to 16M-1 address range, there had been two acceptable methods by which memory adapters could be configured to add their memory to a PC system. One method was by way of the set configuration program and the other was by way of a direct reading and modification of a quantity value describing memory in battery-backed Random Access Memory (RAM).

Disclosure Text (4):
In 32-bit PCs, this value had a maximum of 64MB, not because of any hardware limitation, but simply because that was the maximum number of KB that could be described with only two bytes. However, the method of direct manipulation of battery-backed RAM suffered from more than one disadvantage. Adapters that required their initialization program to exist on the boot-track of a hard disk remained un-configured and was entirely disabled if the system in which they were installed was booted from the floppy drive. Adapters that had their initialization program within ROM on the adapter did not have this same problem, however, the presence of the additional ROM served to further constrict the already crowded space in the 640K to 1M-1 address range. A system into which multiple ones of these adapters were installed would not leave enough non-system memory space available in this address range for ROM's from other adapters. This forced the user to choose between additional memory and other features. A further disadvantage, no matter where the initialization program was based, was the increasing probability that these adapters would have memory that remained disabled in a situation in which a system had non-system memory in the 1M to 16M-1 range, and such an adapter had more than enough memory for the available system memory address. A further limitation was where an adapter initialization program resided, since such adapters could not completely initialize memory existing at address 16M and above. Within the planar ROM existed

the opportunity to cause the processor to enter and return from protected mode whenever necessary in order to reach the memory at higher addresses in order to count, test, and to zero-fill it. Initialization programs existing on the adapter ROM's, or on the hard disk boot tracks, had added difficulty in performing this task. The result had been that the enhanced memory adapter was not entirely initialized if any of its memory existed at addresses 16M or higher. This caused problems for 32-bit operating systems that have tried to use this adapter's memory. In enhanced memory adapters that will not allow any of its memory to exist at addresses 16M or higher, problems can exist. This is because they used the same initialization programs and are configured, after all other adapters are configured, using the set configuration program method. Problems could exist if the user was trying to use this enhanced adapter to install memory greater than 16 MB. This was because the enhanced adapter was useless even in configurations where there was no non-system memory in the 1M to 16M-1 address range. If the user had enough memory on other adapters to get close to address 16M, then this adapter would provide memory only in the address space starting from where the last block of system memory ended and going only as far as address 16M-1. If the user had enough memory on other adapters to go over address 16M, then this adapter would provide no additional memory. Since the adapter must configure after all others, there was no way to move around the memory so as to have it in the lower address spaces where it was willing to function while putting the memory on other adapters in the area starting at address 16M. Due to the limitations of the prior art, the concept described herein is designed to provide a memory adapter that supports both high capacity and proper adherence to the use of the set configuration program when configuring the memory. The design uses 28 of the 29 bits supplied by POS registers 2 through 5 for the purpose of configuring the adapters. Of the 32 total bits made available by this group of four registers, one of the bits of register two is reserved to allow the system to enable, or disable, the adapter, and two of the bits of register 5 are reserved for other functions involving MC protocol. This concept also makes use of sub-addressing of the 2nd and 3rd POS registers, as described in the PC Hardware Interface Technical Reference Manual. This sub-addressing feature does not provide any function that would be required by the concept's memory adapter to function. It is intended only to extend the functions already provided by the 28 bits of register space.

Disclosure Text (5):
The main argument put forward in support of adapters that use initialization programs that modify battery-backed RAM is that the 29 bits that are available for use in the POS registers for configuring a memory adapter are not enough to do the job of a memory adapter. In reality, all that is needed is to optimize the use of the 29 bits. This requires some trade-offs, but not to an extent that makes the solution inoperable. The concept memory adapter operates in two distinct modes: straddle mode, where its memory is split around a block of non-system memory; and contiguous mode, where its memory is arranged as a single contiguous block in a PC address space. The appropriate mode is selected by way of there being a zero, or a non-zero, value placed in a particular set of four of the 29 bits made available by the POS registers, without sub-addressing. Within 28 of the 29 bits made available by the POS registers is the information needed to describe two starting locations for two separate blocks of memory and their lengths, when this adapter is put into straddle mode. The first starting address is described using 8 bits which form a byte to describe the starting address with a one megabyte granularity, and with all of the starting addresses offset by a value of 1M, i.e., hex 00 means starting at address 1M, hex 01 means starting at address 2M, etc. It is assumed that the adapter's memory will never be made to start at address 0, where at least 1 MB of memory is required to be installed on the planar of a PC. The length of the first block of memory is described using another 8 bits, forming another byte, with a 1 MB granularity, and with the values also offset by a value of 1M, i.e., hex 00 means 1 MB, etc. It is assumed that this adapter will have a minimum of 1 MB installed. The second starting address is described with only four bits, forming a nibble, and with a granularity of 16MBs. The values in this nibble are not offset in any way, but are additive on top of where the first block of memory ends in the system's address space.

Disclosure Text (6):
This nibble is meant to describe how many address locations, at 16 MB multiples, to jump before reaching the start of the second block of memory. It is assumed that if this value is non-zero, then some number of address positions will be jumped from the end of the first block of memory to the beginning of the second block. If the first block of memory ends on an address that is on a multiple of 16M, then if the

nibble holds a non-zero value, the second block of memory will start at a number of 16 MB jumps later. The number of these jumps being specified by the value contained within this nibble. In short, if the first block of memory ends at address 32M-1, then if the nibble holds a value of hex 1, the second block of memory will start 16 MBs later at address 48M, or if the nibble holds the value of hex 2, the second block of memory will start 32 MBs later at address 64M, etc. If the first block of memory ends on an address, such that it is not on a multiple of 16M, then if the nibble holds a non-zero value, the second block of memory will start at a number of 16 MB jumps later, but the first jump will not actually be of a size of 16 MBs, but sill simply be a jump to the next address after the first block of memory that is a multiple of 16M. In short, if the first block of memory ends at address 38.5M-1, then if the nibble holds the value of hex 1, the second block of memory will start at address 48M, or if the nibble holds the value of hex 2, the second block of memory will start at address 64M, etc. The length of the second block of memory is described with a last set of 8 bits, forming a 3rd byte and is done in a manner identical to that of the first length using the same granularity and a 1 MB offset. It is assumed that in a straddle mode situation, a minimum of 2 MBs will be installed on this adapter; 1 MB existing before a block of non-system memory in the PC address space and 1 MB after the same non-system memory block.

Disclosure Text (7):
With the 28 bits defined, as above for the straddle mode, the adapter is defined to have the ability to have the starting address of its first block of memory at any address location from 1M to 256M, with from 1 to 256 MBs of memory in that first block. The adapter can then straddle a block of non-system memory as large as 240 MBs, i.e., the second block of memory can start at up to 240 M worth of address space after the end of the first block of memory and be from 1 to 256 MBs in size. When in contiguous mode, a second set of definitions for the same 28 bits is activated if the nibble describing the starting address of the second block of memory holds a value of 0. A zero value indicates that there is no split between the two blocks of memory, i.e., no straddling is to occur. With no straddling between the two blocks of memory, these two otherwise separate blocks effectively become one block. The definitions for the bits forming the two bytes that describe the starting address and the size of the first block do not change between the straddle and the contiguous modes. However, the 8 bits that formed the byte describing the length of the second block of memory in straddle mode take on different purposes, as in contiguous mode, in order to take advantage of an opportunity to achieve greater flexibility.

Disclosure Text (11):
To maintain flexibility and to allow the adapter to make use of future memory technology, the address decode logic is controlled by a simple microcontroller, such as a small 8-bit or 16-bit device, with multiple parallel Input/Output (I/O) ports, although serial linkages should be adequate. The microcontroller would be programmed to receive the POS register values given to it by the PC system during its boot procedure, and based on those values and the program running the microcontroller, it would set up the address decode logic of the adapter to incorporate the appropriate starting addresses and memory block lengths. It is further preferred that the program memory of the microcontroller be a form of electronically eraseable programmable read only memory (EEPROM), and that this EEPROM be made available for reprogramming through the sub-addressing concept of the POS registers. It is not intended that this program be loaded into the EEPROM from the PC's battery- backed RAM every time the PC is booted. What is intended is that within the 64 kilo-words available through the sub-addressing concept, there will exist perhaps 4 or 8 kilobytes worth of address locations that will be locations within the EEPROM for the purpose of allowing the program to be updated from time to time.

Disclosure Text (12):
The reprogrammed feature allows the POS register definitions to literally be altered at some future time so as to allow for new features, or to make it possible to configure the adapter for situations that did not previously exist. This would also allow the adapter to easily incorporate the ability to handle newer technology. It is presumed that the adapter would use memory modules of an industry standard shape, size, and electrical design. Such a standard exists and one of the features that this standard possesses is a set of pins on the module that identifies the capacity and access speed of the module through a set of high and low electrical signals. These signals represent a binary code to which new values have been repeatedly added as larger and faster versions of the modules have been created. As more values are defined for future versions of modules, the ability to reprogram the microcontroller

on the adapter would enable it to recognize the new modules and to set up its configuration as is appropriate in order to fully and properly utilize the memory provided by the modules. * Trademark of IBM Corp.

☐ 3. Document ID: NB9404129

L7: Entry 3 of 19 File: TDBD Apr 1, 1994

TDB-ACC-NO: NB9404129

DISCLOSURE TITLE: Dynamic Link Library Merge Utility

L7: Entry 3 of 19 File: TDBD Apr 1, 1994

DOCUMENT-IDENTIFIER: NB9404129
TITLE: Dynamic Link Library Merge Utility

Disclosure Text (1):
A programmer may need to add some enhanced function onto currently existing functions in an OS/2 Dynamic Link Library (DLL). Normally this would require that the programmer get access to the source code for the DLL, add the new enhanced function, and then rebuild the DLL. The programmer may not have access to the DLL's source code. Disclosed is a way to add new function onto an existing DLL without having to modify the DLL's source code. - The solution is to create a program that will merge the necessary functional enhancements into an existing DLL. DLLs are packaged in an EXE format with an EXE header at the front of the file. The program does the merge by modifying the EXE header in the DLL. The DLL merge utility makes use of several key components in the EXE header: The Segment Table The Imported Names Table -- lists functions imported from other modules The Resident Names Table -- lists functions exported to other modules The utility also uses other tables in the EXE header that support these tables and modifies other fields in the EXE header to complete the merge. The details are discussed in "Details of the DLL Merge Utility." All of the code to support the enhanced functions is built into a separate DLL. For the sake of clarity, we will call the original DLL, the one with the existing functions that are to be modified, the first DLL. The DLL with the enhanced functions will be referred to as the second DLL. - The basic function of the DLL merge utility is to append the code in the second DLL onto the first DLL and then update the EXE header of the first DLL so that it refers to the enhanced functions. The enhanced functions in the second DLL fall into one of three categories. 1. New function 2. Replacement function 3. Front end to an existing function Some functions in the second DLL may be totally new functions. That is, they are functions that do not exist in the first DLL. When the second DLL is built, the new functions are registered as non-ordinal exports of the DLL. Their entry points will be published in the Resident Names Table in the EXE header of the second DLL. - The DLL merge utility scans the Resident Names Table of the second DLL. For each entry in the table it scans the Resident Names Table of the first DLL to find a matching entry. Entries for new functions in the second DLL will not appear in the Resident Names Table of the first DLL. All the utility needs to do for entries for new functions is copy the information from the Resident Names Table entry in the second DLL to the Resident Names Table of the first DLL. This new entry is appended onto the end of the Resident Names Table of the first DLL. This action effectively creates an export entry in the first DLL for the new function. - Other functions in the second DLL may

number. o Imported Name This is a reference to an entry point in another module which is being imported by name. o Entry Table This table contains the segment, offset and type of each entry point within the EXE file. The entry points are bundled together by segment. The number of bundles in the Entry Table varies from one bundle to many. o Resident Names Table This table lists all the exported entry points that were not assigned ordinal numbers. Each entry in the table is a counted string (that is, a byte that contains the length of the string followed by the string itself), followed by a one-based index into the entry table. o Imported Names Table This table contains the names of the imported functions and names of modules that contain imported functions. Each entry in the table is a counted string. - Here are the steps that the DLL Merge Utility takes to merge the functions in the second DLL into the first DLL. Read the two DLLs into memory. DO for each segment in the second DLL. - DO for each entry in the segment's relocation table. - SWITCH on the relocation type. - Internal Fixup -- This entry refers to another segment within the second DLL by way of an index into the Segment Table. The segments will have different indexes after they are merged into the first DLL. Dynamic Link Library Merge Utility Update the segment number in the entry. The segments in the second DLL will be appended after the segments in the first DLL. Therefore, the new segment can be obtained by simply adding on the number of segments in the first DLL. - Import by Ordinal -- The import by ordinal is based off of a name in the import names table in the second DLL. It must be changed to be based off of a name in the first DLL since the EXE header of the second DLL will go away in the merge. Look up the name for the import in the second DLL's Import Names

Disclosure Text (2):
Table. Scan the first DLL's Import Names Table to find an entry that matches the one in the second DLL. Change the base of the import in the relocation entry to the base used in the first DLL. - Import by Name -- The only entries that are imported by name should be the ones that are used by the front end functions to which the front end will eventually chain. Look up the name for the import in the Second DLL's Import Names Table. - Find the matching export entry in the first DLL and extract the entry point information, i.e., segment number and offset. - Convert the relocation entry from an import by name to an internal fixup using the information obtained from the export entry in the first DLL. DO for each entry in the Import Names Table in the second DLL. - Find the matching entry in the first DLL's Resident Names Table. - Zap the Resident Names Table entry to a different name. DO for each entry in the second DLL's Resident Names Table Get the information on the entry point from the Entry Table. - IF there is an entry with the same name in the first DLL's Resident Name Table, THEN Overwrite the Entry Table entry in the first DLL with the information on the entry point in the second DLL. - ELSE Append the entry to the first DLL's Resident Names Table. - Append the entry point to the first DLL's Entry Table. - Append the segments in the second DLL to the first DLL. That is, append everything from the second DLL except its EXE header. When appending the segments to the first DLL the segments must start on the border of an alignment block. The size of an alignment block is obtained from the EXE header. The standard alignment size is 512 bytes. Update the new file size and check sum in the EXE header of the first DLL. Write the first DLL back to disk.

☐ 4. Document ID: NN9311629

L7: Entry 4 of 19 File: TDBD Nov 1, 1993

TDB-ACC-NO: NN9311629

DISCLOSURE TITLE: National Language Support Enablement for Culture-Specific Operations

L7: Entry 4 of 19 File: TDBD Nov 1, 1993

DOCUMENT-IDENTIFIER: NN9311629
TITLE: National Language Support Enablement for Culture-Specific Operations

Disclosure Text (1):
This document contains drawings, formulas, and/or symbols that will not appear on line. Request hardcopy from ITIRC for complete article. Figure 1. Organizational Structure Disclosed is an architecture for performing culture specific operations on parameters that are inserted into text strings as part of National Language Support (NLS) enablement of a software product. Parameter types include but are not limited to items such as the following: o Time of Day o Date o Character Direction o Monetary Values o Character Shaping o Cursiveness o Weights and Measures o Double Byte Character Set Support The architecture is described in terms of its structural organization and operation. Fig. 1 depicts the structure of the support for the culture specific operations. It is based on the following elements, each of which is described in more detail in subsequent sections. o Culture Specific Exits (CSE) o Culture Specific Tables (CST) o Culture Specific Exit Interface (CSEI) o Element Integration Code (EIC) Culture Specific Exits (CSE) are object or load modules maintained in a library of executable code. Each CSE performs a unique culture specific operation. Operationally they are combined as necessary but functional separation is maintained. Note: The architecture allows for exits to perform other types of operations upon the substitutable parameters such as conversion from one code page and character set to another or table translation of the parameters. - Culture Specific Tables (CST) are used to drive and control the execution of the various CSEs. These tables reside in a source type library such that each member constitutes a table to drive the CSEs for a specific national language. - The tables are designed such that as new parameter types are identified that require CSE support, they can be easily expanded. When the need to implement another national language is required, all that is needed, provided that the necessary CSEs exist, is to build a new CST to drive the invocation of the applicable subset of the set of all CSEs. - The CST consists of an 80 byte character record for each parameter type. The format is self documenting as each record consists of two keyword(value) parameters as shown in Figure ?? on page 26 below. The TYPE keyword identifies the parameter type followed by a predefined encoded value (see "Parameter Typing"). The EXITS keyword identifies one or more CSEs to be invoked, in order, for the specified parameter type. None, one, or multiple exits may apply for any single parameter type. - It is recommended that a naming convention be used for table names that is consistent with one used for other related files such as messages and panels. In this way, the name of the associated CST can be readily determined. A national language code should be a part of the name. For example, AP is the code for a product, MSG/PNL/CST represents the file content/type, and 'nl' represents a code assigned to a specific language. - o Message File = APMSGnl o Panel File = APPNLnl o Custure Specific Table = APCSTnl The Culture Specific Exit Interface (CSEI) is the interface for passing parameters to and receiving results back from the CSEs. The CSEI is based on the following parameters: o Input Parameters String Address Address of the beginning of the text string Insertion Address Address of the point within the text string where the parameter is to be inserted (i.e., where the symbolic variable, such as '&1', that is to be replaced, is located within the text string). - String CCSID The coded character set identifier for the basic text string. This identifies the encoding scheme, character set, and code page used to represent the data. - Parameter Address Address of the beginning of the unmodified parameter that is to be inserted into the text string Parameter Length Length of the unmodified parameter that is to be inserted into the text string Parameter CCSID The coded character set identifier for the parameter. - o Input/Output Parameters Parameter Address Address of the beginning of the modified parameter that is to be inserted into the text string. This value may or may not be the same as the input parameter address. If it is necessary for the CSE to increase the size of the parameter, the value would be modified upon return. - Note: On input, is the address of an area in memory where the parameter may be returned if additional space is required. - Parameter Length Length of the modified parameter that is to be inserted into the text string. It may or may not be the same as the length of the unmodified parameter. - Note: On input, is the maximum length of the parameter that can be returned, (i.e., the size of the area in memory pointed to by the parameter address

is to be based on a different calendar, the new date should be calculated prior to converting to the format in which the date is to be presented. If it is necessary to call multiple CSEs, the modified parameter from the first becomes the unmodified parameter for the second and so forth. - After all applicable CSEs have been invoked in sequence for a parameter, the EIC replaces the symbolic variable with the final modified parameter, shifting any characters in the basic text string right as necessary. This is done prior to scanning for and processing the next symbolic parameter.

☐ 5. Document ID: NN910294

L7: Entry 5 of 19 File: TDBD Feb 1, 1991

TDB-ACC-NO: NN910294

DISCLOSURE TITLE: Memory Partition Table for Multiprocessor Optimization.

L7: Entry 5 of 19 File: TDBD Feb 1, 1991

DOCUMENT-IDENTIFIER: NN910294
TITLE: Memory Partition Table for Multiprocessor Optimization.

Disclosure Title (1):
Memory Partition Table for Multiprocessor Optimization.

Disclosure Text (1):
- Disclosed is techniques for optimizing performance of a multiprocessor system in which the memory may be partitioned. The approach is to employ a memory partition table to record the usage of individual memory partitions by individual processors. - In certain computer systems the (main) memory may be partitioned (e.g., into 1 megabyte partitions). Each partition may be dynamically assigned to be used by particular process/system under certain hypervisor control. Furthermore, in a multiprocessor environment, a particular underline process/system may be affixed to run on particular processor(s). Under this partitioned environment, the concurrently running systems rarely share memory data. Data coherence control is clearly an important factor in multiprocessor design. With the partitioned system structure, we may optimize the performance with the knowledge of specific usage of a memory partition by particular processors. - Assume the (main) memory is partitioned into p partitions {Mi 1&i&p} and that there are n processors {Pj 1&j&n}. We will consider a partition table (PT), which may be viewed logically as two-dimensional bit matrix. The bit PT(i,j) represents the knowledge of accessibility of partition Mi by processor Pj. When bit PT(i,j) is ON (=1), the multiprocessor control will assume that Mi has recently been accessed by Pj. - Certain hypervisor-type system control dynamically (but infrequently) grants and deletes the authorization of data accessing to particular memory partition(s) by a particular underline process/ system. Similarly, the system control dynamically (and infrequently) assigns the set of processor(s) that a particular underline process/ system can run on (which we call the processor affinity). - We will illustrate the ideas with a particular usage of PT. Initially, all bits are OFF (=0). Whenever Mi is accessed by Pj (e.g., upon a cache miss), the bit PTi,j is turned ON. Whenever the authorization of access to Mi by a process/system is deleted, the hypervisor control will (at proper point) do the following, using special command(s), for each Pj that PT(i,j) is ON: All data change

form Pj are reflected in the memory. All cache lines of the partition Mi in the private cache(s) of Pj (if applicable) are invalidated there. Turn the bit PTi,j OFF. - Now we illustrate how the PT table may be used to facilitate mulitprocessor cache design. When a processor Pj modifies a cache line L belonging to Mi, it is necessary to have L invalidated from remote caches properly. In certain systems (e.g., IBM/3090) copy directories of processor caches are maintained at the storage control (SC) in order to identify the target caches for such XI-invalidates. However, in some designs such information of private cache contents may not be available, and hence the XI-invalidate of L may need to be broadcasted to all remote caches. With the PT facility, such XI-invalidates only need to be signaled to each remote processor Pk such that PTtheyi,kÙ is ON. - Although a specific application of PT has been illustrated in terms of cache XI-invalidate processing, other similar applications may be derived. Similar filtering of cache invalidation may be used for other types of memory updates (e.g., channel stores). Similar variations may also be employed to filter activities for processing of TLB entry invalidate and storage key changes. - In the illustrated example, a PT bit is turned OFF only upon the drop of memory partition authorization to a process/system. For various designs it may be useful to turn PT bits OFF at different conditions (e.g., upon cache purge, or upon recovery). It is also possible to have PT bits turned ON using special commands (e.g., by the hypervisor upon granting of access to memory partitions), in which case the PT may also serve as a vehicle for memory access protection verification. Finally, the PT may be implemented with special circuits (e.g., at SC) or as part of conventional memory data (e.g, in special system area).

☐ 6. Document ID: NB9011291

L7: Entry 6 of 19 File: TDBD Nov 1, 1990

TDB-ACC-NO: NB9011291

DISCLOSURE TITLE: Optimized Drawing of Filled And Unfilled Circles in a Two-Dimensional Graphics System.

L7: Entry 6 of 19 File: TDBD Nov 1, 1990

DOCUMENT-IDENTIFIER: NB9011291
TITLE: Optimized Drawing of Filled And Unfilled Circles in a Two-Dimensional Graphics System.

Disclosure Text (1):
- Most algorithms are quite efficient in drawing large unfilled circles. However, in most cases, the circles appearing on the screen are quite small and in each one of the algorithms the time to calculate the points on the circle can be as much as 90% of the total time taken to render the circle. To improve this situation a customized look-up table can be used to reduce the calculation time to a minimum. - To optimize the drawing of filled circles, a version of the Bresenham algorithm is used. - Both of these techniques are discussed in this article. - Circle Algorithms In reviewing the literature they1,2,3,4Ù for the implementation of drawing circles in graphics systems, it becomes apparent that the only algorithm that minimizes errors in finding the points on the perimeter of circle is the Bresenham algorithm. This algorithm computes the points on the perimeter one by one starting from some point and proceeding until the total circle is drawn. The Bresenham algorithm is described

☐ 7. Document ID: NN8806348

L7: Entry 7 of 19 File: TDBD Jun 1, 1988

TDB-ACC-NO: NN8806348

DISCLOSURE TITLE: Parallel Data Partitioning of Shared Memory Computers, Using Fetch and Add With Block Transfers

L7: Entry 7 of 19 File: TDBD Jun 1, 1988

DOCUMENT-IDENTIFIER: NN8806348
TITLE: Parallel Data Partitioning of Shared Memory Computers, Using Fetch and Add With Block Transfers

Disclosure Title (1):
Parallel Data Partitioning of Shared Memory Computers, Using Fetch and Add With Block Transfers

Disclosure Text (1):
- A technique is described whereby multiple processors can, in parallel, partition a data array that is stored in shared memory, into multiple data arrays that are also stored in shared memory. Fetch and add concepts are utilized in a parallel partitioning algorithm, so as to avoid processor synchronization delays. Also, block data transfers are used to minimize interconnection network delays. Typically, parallelism is used in data partitioning to improve performance of database computer systems. Fundamental operations of relational database systems are designed to partition data arrays into multiple disjoint arrays or subarrays, so as to achieve improvements in performance such as: $ Quicksort - where the array is split into two subarrays, depending on whether the key value is either less than or greater than or equal to a partition element. - $ Bucketsort - where the array is split into multiple buckets, or arrays, such that all the key values in a bucket lie between two specified values. - $ Hash-partitioned Join Algorithms - where the array is partitioned on the basis of a hash value. As highly-parallel shared memory computers have become available they1Ù, efficient algorithms have been developed to exploit these fundamental capabilities. The data partitioning phases of the algorithms used can generally be described as follows (for example, see they2Ù): Assume that there is an array {X(i),i = 1, ... ,N} in global memory that is to be partitioned into K arrays {Y(k,*),k = 1, ... ,K} which is also stored in global memory. The partitioning function is denoted by P, in that if P(X(i)) = k, then X(i) is to be stored in the array Y(k,*). Global shared counters I and {J(k),k = 1, ... ,K} are defined and initialized to one. Each processor defines XL, IL, JL and KL to be local variables. In parallel, each processor repeatedly executes the following operations (in pseudo Pascal): IL=F&A(I,1) Allocate an element from X (if IL > N, then stop XL=X(L) Copy the element into local memory KL=P(XL) Determine the partition to which the element belongs JL=F&A(J(KL),1) Allocate an element from the appropriate global partition array Y(KL,JL)=XL Store the element into the appropriate global partition array The number of fetch and adds (F&A) can be reduced by generalizing the algorithm to allow processors to allocate more than one element at a time from X by using F&A(I,M), where M > 1. However, two memory access delays across the interconnection network are incurred for each element of X, assuming that processors must wait on stores. Even if X is cacheable, problems may occur because two

Prototype (RP3): Introduction and Architecture," Proceedings of the 1985 International Conference of Parallel Processing. 2 A. Norton, "Parallelization of Quicksort Using Fetch-and-Add," 1986 IBM Research Report RC 11884. T. J. Watson Research Center, Yorktown Heights, New York 10598. 3 P. A. Franaszek, "Path Hierarchies in Interconnection Networks," IBM Journal of Research and Development (January 1987). 4 "Parallel Equi-Join Algorithm for Large Relational Data Base Operations," IBM Technical Disclosure Bulletin 30, 361-365 (October 1987).

☐ 8. Document ID: NN87081102

L7: Entry 8 of 19 File: TDBD Aug 1, 1987

TDB-ACC-NO: NN87081102

DISCLOSURE TITLE: Font Organization for Multiple Performance Configurations

L7: Entry 8 of 19 File: TDBD Aug 1, 1987

DOCUMENT-IDENTIFIER: NN87081102
TITLE: Font Organization for Multiple Performance Configurations

Disclosure Text (1):
- This article describes a baseline character generator that can be used to generate a raster image of a page from a memory that contains a coded and ordered representation of the page. More specifically, it describes a baseline character generator which has two performance configurations. The slower print speed configuration allows logic to be deleted without redesigning several pieces of the logic. The system shown in Figs. 1 and 2 provides for either a one-scan or a two-scan configuration for the font, font aligner logic, and the font address generation logic. Basically, the two-scan configuration processes two parallel scans of pel data at one time by duplicating the font data aligner logic and the scan buffer memories, and by reading the font data twice as wide per fetch (i.e., addressing cycle). The font address generation logic generates font addresses in the appropriate order depending on the configuration of cards which are populated. A signal "onescan*" is generated on the font and scan buffer cards by the wiring on the card(s). The signal is readable by the processor and is used to control the font address generation logic. The character generator can print in 8 scan orientations, as shown in Figs. 3 and 4. The case numbers which are shown in the figure relate character orientation to scan direction orientation. For a machine with a fixed scan direction in relation to the long edge of the paper, the case numbers relate character orientation to paper orientation. If the machine feeds paper in two orientations as some printers do, the case numbers relate character orientation to paper orientation by the two separate but related methods. The case numbers are shown in parentheses in Fig. 3, and the binary representations used in the print I/O command are shown in quotes. The following is an overview of the character generator operation. The character generator consists of 4 memories which are addressable by the control unit: Font Address & Escapement (A/E) Page Buffer (PB) Column Position & Escapement (CPE) Font Memory The font memory contains the raster dot (pel) patterns of all printable characters with one bit of storage for each dot or pel. A logical "1" appears as a dark pel. The control unit can read and write this memory as halfwords (16 bits) or as bytes. Address and Escapement Memory The address and escapement memory is a pointer table consisting of one entry for every character

When all the text is processed, the control unit is interrupted and the character generator is placed in transparent mode by the hardware. Character Generator Operation The character generator is pipelined and all operations are performed simultaneously but on different characters. This is the sequence as a single character goes through. (Refer to Figs. 1 and 2.) 1. When the print command is issued, the character generator reads the first CPE location. 2. The CPE data is used to address the page buffer and determine which character is to be processed. 3. The page buffer data which is obtained is used to address (i.e., as an offset) into the A/E. 4. The character size and font reference address information (in the A/E) along with the current escapement from the CPE are used to determine the font address. 5. The new current escapement and page buffer address are computed and written back into the CPE. The current escapement is decremented with each pair of scans of a character being processed. The page buffer address entry in the CPE changes only when the last scan of the character is processed. 6. The font address is used to read pel data, processed and compacted, from the font which is later stored in an input scan buffer. 7. The preceding operations are repeated until the input scan buffer is full. At this time, the full-scan buffer is swapped with an empty (output) buffer.

☐ 9. Document ID: NN87081085

L7: Entry 9 of 19 File: TDBD Aug 1, 1987

TDB-ACC-NO: NN87081085

DISCLOSURE TITLE: Underscoring With Multiple Thickness Capability As a Function of Scan Direction and Print Orientation

L7: Entry 9 of 19 File: TDBD Aug 1, 1987

DOCUMENT-IDENTIFIER: NN87081085
TITLE: Underscoring With Multiple Thickness Capability As a Function of Scan Direction and Print Orientation

Disclosure Text (1):
- This article describes an underscoring feature of a baseline character generator that can be used to generate a raster image of a page from a memory that contains a coded and ordered representation of the page. The design implements underscoring on a baseline character gener ator which prints in 8 scan directions, and has the ability to print variable height and width characters. The design allows underscore (and/or double underscore) to be associated with each character regardless of which of the 8 print scan orientations are being used. Underscore is considered in two different printing modes: normal and rotated. A normal underscore is an underscore which is perpendicular to the scan direction while a rotated underscore is parallel to, or in the, scan direction. These two types of underscore are controlled by the same logic pipeline but are implemented as pels in two separate sections of the logic. Normal underscore is always put at the bottom of the first font fetch of a character regardless of which of the 4 normal scan modes is in use. This underscore is turned into pels in the font data aligner chip. Rotated underscore is forced into different locations within the character box depending on which of the 4 rotated scan modes is in use. Pels are generated on the font data aligner chip in a different way than the normal underscore, and timing for the rotated underscore is

perpendicular to scan parameter. For the character shown in Fig. 11, the parallel to scan size (x) would be 128 O X O 160 pels (i.e., _ 4 O (X/32) O 5 slices). - _ In Fig. 12, the "Xs" are in the locations pointed to by the font reference address in the A/E memory. The character above is a large rotated orientation P. Each horizontal set of slices of this character is 32 pels tall with a width which is the A/E's character size perpendicular to scan parameter. The width of the entire character (vertical size in Fig. 12) is the A/E's character size parallel to scan parameter. For the character shown in Fig. 12, the parallel to scan size (x) would be 96 O X O 128 pels (i.e., 3 O (X/32) O 4 _ _ slices). Fig. 13 shows the position of a forced black pel for the 16 combinations of page buffer underscore control bits. It also shows the various options of underscore that are available in hardware. The "Xs" represent pels which are forced black if the underscore bits in the page buffer are set, as shown. The pel number is the position of the forced black pel with relationship to the bottom of the character box. (Pel number 1 is the bottommost pel in the character box.) Underscores can also be implemented by putting a short character line between text lines if the underscore options are not what is needed. This option uses up some of the lines that can be printed, and so reduces the 180 lines per page limit to one-half or 90. Underscore can be supported for all line heights which are large enough to include the underscore bits. (See Fig. 13.) Line height is the distance from the bottom of one character box to the bottom of the next character box. Lower underscore will be in the bottom of the character box (with respect to character orientation) for both normal and rotated orientation characters. Upper underscore is separated from the lower underscore by various numbers of white pels. Double underscore is done by printing both upper and lower underscore. The bottom of double underscore lines up with regular underscore.

☐ 10. Document ID: NN86091494

L7: Entry 10 of 19 File: TDBD Sep 1, 1986

TDB-ACC-NO: NN86091494

DISCLOSURE TITLE: Extending the Addressing Capabilities of the IBM Series/1 to 32 Bits

L7: Entry 10 of 19 File: TDBD Sep 1, 1986

DOCUMENT-IDENTIFIER: NN86091494
TITLE: Extending the Addressing Capabilities of the IBM Series/1 to 32 Bits

Disclosure Text (1):
- A technique is described whereby the total logical addressability of the IBM Series/1 is extended from 20 bits (1 megabyte) to 32 bits (4 gigabytes). The extension divides the total two gigabytes of addressing capability into 256 address spaces, each having an addressing capability of from two kilobytes to 16 megabytes. The technique described herein allows the current 16-bit IBM Series/1 to not only support existing software programs, but to enable new software programs having 24-bit addressability to run concurrently with the current programs. In addition, the concept supports all existing input/output attachments. The extension supports 16 megabytes of real storage, all of which can be addressed using real, non-translated addresses. In prior art, only one megabyte of real storage was supported, of which only the low-order 64 kilobytes were addressable using real

addresses. Described herein are the various mechanisms and techniques used to implement the extended addressing function. For detailed descriptions of the major operational mechanisms, reference should be made to the articles on pages 1474-1493 of this issue. The following eleven items represent the changes and additions made to the IBM Series/1 architecture to provide for the extended addressing capability: 1. The number of address spaces is increased from 16 (four- bit keys) to 256 (8-bit System Identifier theySIDÙ). 2. Individual address spaces are increased from 64K bytes (16-bit address) to 16M bytes (24-bit address). 3. Real storage addressability, with the Translator disabled, is increased from 64K bytes to 16M bytes. 4. Processor segmentation registers are replaced by segment tables, which reside in real memory. 5. The eleven-word level status block theyLSBÙ (22 bytes) is increased to eleven double words (44 bytes). 6. The processor status word (PSW) is increased to 32 bits. 7. The level status word (register) is increased to 32 bits. 8. Bit 09 in the PSW is designated to indicate the operational mode of the system. When on, it indicates extended mode. When off, it indicates compatibility mode. 9. Bit 21 in the LSR is defined to indicate the mode of execution for the program resident on level. When on, it indicates extended mode. When off, it indicates compatibility mode. 10. An optional address translation cache is provided to enhance performance during storage accesses. 11. Some instructions have been redefined and others have been added to enhance the management of the addresses as a double word data type. A significant feature of the extended addressing capability is the way address space is managed. This involves two types of address spaces: Real and Logical. Programs executed using Logical addresses are translated dynamically, by the hardware, to Real addresses during run time. When the translator is off, programs are executed using Real addresses with the capability of accessing 16M bytes. When in extended addressing mode, storage resident segment tables are used to map address spaces rather than using the prior-art method of hardware-implemented segment registers. The use of segment tables reduces the mapping costs, since a maximum system in the prior art would have required two million 4-byte registers. Also, using the prior art of segment registers, an address space is always fixed at the maximum size, whereas, using storage resident segment tables, each address space can vary from 2K bytes to 16M bytes. To support the segment tables, an address space array hardware facility is provided to provide an entry for each address. Each entry contains a pointer to specify the beginning of the segment table and a number specifying the current length of the entries. The address space array has the ability to map 256 segment tables. Each segment table has the ability to map an address space of from 2K bytes to 16M bytes. Each segment table entry has the ability to point to a 2K-byte segment. The total system logical address space is divided into 256 sub spaces, uniquely identified by an eight-bit SID (space identifier). The SIDs are managed as part of the run time context of a program. Each address space can be up to 16M bytes in size. During execution, the active level has two SIDs residing in the extended level status block (ELSB). During the generation of an extended effective address, the processor has the ability to check the program. If a program check does not occur, the processor presents the effective address to the translator. The translator selects a system identifier from the active extended level status block where it is concatenated with bits from the effective address and presented to storage as a 32-bit system logical address. The translator then performs the following function: Using the active system identifier, the address space array is accessed for the associated segment table origin address and the segment table limit. If no program check occurs, the appropriate segment table entry bits are concatenated with the appropriate bits of the system logical address to form a 24-bit translated real address to be used to access storage. The address translation requires that two storage accesses be made for each instruction or opened access. This instruction execution could be unacceptable for certain applications. Therefore, a cache mechanism is offered as an optional feature. Previously translated addresses are cached so as to eliminate the additional accesses to storage for a large percentage of store requests. When a cache is implemented, the number of entries in the cache is limited to 8K bytes by the 13-bit logical segment address. However, the number of entries and the levels of associativity are the choice of the user. The cache is transparent to programming and the contents of a cache entry properly reflect the contents of a cache segment table entry, provided that the table entry was modified using only the redefined set segment register instruction. The set segment register instruction, operating in redefined format, is used by the address space management programs for supporting the extended addressing capabilities. Interrupt handling in extended mode is performed architecturally similar to the way it is performed in compatibility mode with the exceptions explained on page 1489. The implementation of extended addressing required certain checks to be imposed so as to insure proper handling of the addresses. Checks such as invalid effective addressing, invalid address space,

segment length exceeded, segment table exceeds memory capability, invalid segment and translated address exceeds memory are examples of the checks built into the concept. When generating an effective address for a jump instruction, a program check occurs if there is an addition to the displacement field. The implementation of extended addressing required certain changes to the classes of instructions when executing programs in extended mode. For example, double shift instructions use a single 32-bit register instead of two contiguous 16-bit registers. All register to register instructions use 32 bits and indicator settings reflect the 32-bit result. All branch instructions are extended to thirty-two bits. Register to storage word instructions are performed by using the least significant word, rather than byte, of the register specified, and encompass operations such as: Move Word, OR Word, Reset Bits Word, Exclusive OR Word, Compare Word, Move Word and Zero, Add Word, Subtract Word, Push/Pop Word, Multiply Word and Divide Word. Multiple register to storage instructions remain the same as in compatibility mode except for two instructions: Load multiple and branch which is incremented by four, and Store multiple where the last register stored is set to the address of the low storage end of the block on the stack and incremented by four. System register to storage instructions is changed so that the set segmentation register instruction is used by address space management programs for supporting extended addressing such that the contents of double word storage locations, specified by the effective address, are loaded into the target facility specified by the contents of the register specified by the facility address field. Whenever address space management changes take place in a segment table, entries must be updated before any program allocated to an address space can proceed. The following instructions are implemented to perform the updating functions: Set Level Block instruction, Set Address Key Register instruction, Copy Processor Status Word instruction, Copy Segmentation Registers instruction, Copy Level Block instruction and Copy Address Key Register instruction. New extended mode instructions are added: Add Double Immediate - this instruction operates the same as Add Word Immediate except that an overflow indicator is turned on if the sum is less than -231 or greater than +231 - 1. If an overflow occurs, the result will contain the correct low-order 32 bits of the sum. If one or more words of the instruction pointed to by the translated instruction address are outside the fitted storage size of the system, the instruction is suppressed and a program check interrupt occurs. Compare Double Immediate - this instruction operates the same as Compare Word Immediate except that the overflow indicator will be turned on if the difference is greater than +231 - 1 or less than -231 . Some additional instructions include Move Word Immediate, Jump Long Unconditional - this instruction provides for bit 16 of the word displacement field to be propagated to the left by 15-bit positions and a zero is appended at the low-order end resulting in a 32-bit double word. This value is added to the updated value of the instruction address register, and the result is stored so as to be the next instruction to be fetched. Jump Long - On Condition, - On Not Condition, - On count, - and Link, - these instructions are similar to Jump Long Unconditional except conditions are imposed for the long jump. Move Double Short (Load) - this instruction allows the six-bit unsigned integer in the Word Displacement field to be doubled in magnitude and added to the contents of the register specified by the field to form the effective address. The contents of the double word in storage specified by the effective address are loaded into the register specified. Move Double Word Short (Store) - this instruction allows the six-bit unsigned integer in the Word Displacement field to be doubled in magnitude and added to the contents of the register specified by the field to form the effective address. The contents of the double word in storage specified by the effective address are stored into the storage location specified. Kernal Call - this instruction is under the control of system programming and allows the Instruction Address Register to be incremented by two. To support extended addressing, additional channel lines were added. The following chart shows the current and extended lines which make up the extended Series/1 channel: ***** SEE ORIGINAL DOCUMENT ***** Referring to the channel lines, the following describes their usage during data processing and

Disclosure Text (2):
cycle steal transfers: a) The 16 address bus lines are bidirectional and are used by the processor, in conjunction with a six-line extended address bus and a three-line key bus, to present a 25-bit address to storage during all storage accesses when the system is operational in extended addressing mode. b) The data bus line is an 18-line (16 data, 2 parity) bidirectional bus. It is driven by the processor during storage write sequences and by storage during read sequences. On write sequences, it must be valid prior to the activation of the select tag line, and on read sequences, it must be valid prior to the activation of the ready tag line. It must remain valid on write sequences until the ready tag is activated, and on read sequences, it must

be valid until the select tag is de-activated. c) The cycle input indicator is a bidirectional tag line used by the processor and I/O during storage accesses. It specifies whether the access is to read or write storage. d) The cycle byte indicator is also a bidirectional tag line used by the processor and the I/O during storage accesses to specify whether the data transfer is a byte or a word. When a byte transfer occurs, the address on the address bus is even and resides in data bus bits 0-7. When the address is odd, the data byte resides in data bus bits 8-15. Both bytes maintain good parity during byte transfers. e) The status bus is driven by storage during storage access sequences to provide information back to the processor or I/O relative to the success or failure of the accesses. f) The condition code/key bus is a three-line bidirectional bus used by the processor in conjunction with the address bus and the extended address bus to present a 25-bit address to storage during all storage accesses. g) The extended address bus is a six-line unidirectional bus used by the processor in conjunction with the address bus and the key bus to present a 25-bit address to storage during accesses and is used only when the system is in extended addressing mode. The timing specifications for this bus are the same as those for the address bus. h) The double word tag line is used by the processor during all storage access sequences, when the system is in extended addressing mode, to specify that a double word is being transferred. i) The select tag line is unidirectional and is used in conjunction with the ready line. It provides a set of interlocked non-symmetrical clocks for synchronizing the extended bus sequences. It is activated by the processor after activation of the address bus, key bus, extended address bus and the cycle indicator line. On write accesses, the data bus must also be activated prior to select. Depending upon whether the data transfer required is byte, word or double-word, the cycle byte indicator line or the double word line may also have been activated. Any time delay between activation of these lines and the select line is sufficient to guarantee that they will be valid at the output pins of the processor. j) The ready tag line is also unidirectional and is used in conjunction with the select line for synchronizing the extended bus sequences. It is activated on a read sequence after the activation of the data bus and the status bus. On write sequences, only the status bus is activated prior to the ready bus activation. The ready line and the active buses remain valid until the de-activation of the select line. When in extended addressing mode, a significant increase in the number of double word storage accesses will be required by the processor. With only a word data bus, the double word transfers will require two complete storage accesses or a single storage access and two bus sequences. In either case, the performance impact could be unacceptable. Also, if an address translation mechanism external to the processor, such as a channel attached facility, is implemented, there is a need for a separate addressing path to storage. This separate path allows the translator to access the segment tables. Therefore, to support systems requiring high performance and/or with address translators which are not integrated into the processor, an optional storage bus containing 28 lines is provided. This extended address storage bus consists of 24 address/data lines, and one each of a storage select line, a translate select/acknowledge line, an acknowledge select line and a data valid line. The following describes the use of the storage bus lines: a) The address data bus consists of 24 lines to transfer both data and addresses. Eighteen lines are bidirectional and are used during double word reads and writes to transfer 16 data bits plus two bits of byte parity. During all address translations, the translator uses the entire 24 bit real address for accessing a segment table entry. After translation, the translator uses all 24 lines to present a real byte address to storage for the required data access. During double word write sequences, high-order data is presented on this bus by the processor. It must be valid prior to activating the data valid tag line and must remain valid until the ready line on the Series/1 channel becomes active. On double word read sequences, high-order data is presented on this bus by storage. It must be valid prior to activating the data valid tag line and must remain valid until the select line on the Series/1 channel becomes active. When the translator is driving the bus to present either an address for a segment table entry or a translated address, the bus must be valid prior to the activation of the translate select/acknowledge or the storage select tag lines, respectively. The bus remains valid until the activation of the acknowledge select tag line. b) The storage select tag line is unidirectional and is activated by the translator after activation of the address/data bus. It will remain active until acknowledge select becomes active. c) The translate select/acknowledge tag line is also unidirectional and is activated by the translator when accessing a segment table entry, after activation of the address/data bus. It remains active until the data valid tag line becomes active and the segment table entry has been registered from the address/data bus. d) The acknowledge select tag line is unidirectional and is activated by storage after the storage select or the translate select/acknowledge line has been activated and the

address on the address/data bus has been registered. It remains active until the storage select or the translate select is deactivated. e) The data valid tag line is bidirectional and is activated by the processor during data transfer or a double word storage write sequence. It is activated after the address/data bus is valid. It remains active until the ready line on the Series/1 channel becomes active. The line is activated by storage after presenting the segment table entry on the bus during translation sequences or placing data on the bus during double word read sequences. It is activated after the address/data bus is valid and remains active until the select line on the Series/1 channel becomes inactive or until the translate select/acknowledge line becomes inactive.

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☐ 11. Document ID: NN86044768

L7: Entry 11 of 19 File: TDBD Apr 1, 1986

TDB-ACC-NO: NN86044768

DISCLOSURE TITLE: Recomputing Cyclic Redundancy Code Check Bits

L7: Entry 11 of 19 File: TDBD Apr 1, 1986

DOCUMENT-IDENTIFIER: NN86044768
TITLE: Recomputing Cyclic Redundancy Code Check Bits

Disclosure Text (1):
- In some computer subsystem architectures, all or part of the data from a direct-access storage device is temporarily stored before being transmitted to the system. To assure data integrity, Cyclic Redundancy Code (CRC) check bits are typically appended at the end of the data field by the transmitting end, and stored at the receiving end. If errors are detected, an attempt is made to correct them before sending them to the channel. However, once any part of the field is changed because of correction or updating, the CRC bits are no longer valid, and have to be updated to reflect the changed data. In the past, CRC bytes have been regenerated for a given data field by clocking the entire data field through CRC hardware. In some cases, the data field clocked through the CRC hardware comprised the first changed byte through the last byte of that field, where a byte is a unit of data without specific bit length. The amount of time required to recompute the CRC was directly proportional to the physical position of the data bytes changed within the field. Thus, it takes more time to recompute the CRC if the changed bytes are at the beginning of the data field than if the changed bytes are near the end of the field. In accordance with the new method described here, CRC check bits for data which have been updated are themselves updated without having to clock the data through a CRC generator. As the length of the data field becomes relatively large, improvement in execution time becomes more significant. Procedurally, the original and updated data fields are added (modulo 2). The resulting data field has three parts: an initial part containing zero bytes, a middle part with nonzero bytes (where the field has been updated), and a tail end of zero bytes. Next, the (partial) CRC of the second part (the nonzero bytes) is generated. Using Galois Field multiplication, the partial CRC is multiplied by (T**n), where T is the generator polynomial in the form of a square matrix (as discussed below), and 'n' is the number of zero bytes in the tail end. Finally, the result is added to the original CRC to produce the check bits of the updated data field. The process of multiplying the partial CRC by (T**n) replaces the need for streaming the data through the generator. By breaking 'n' down into components which are stored, the task is now reduced to multiplying the partial CRC by the various factors of (T**n), which makes the implementation fairly straightforward. The CRC generator is the hardware implementation of a set of equations represented in the form of a square matrix. If CRC of the second part be C(r), the remainder, after passing the first zero byte through the generator, is C(r+1). Then, C(r+1) = T C(r), where T is generator polynomials in the form of a square matrix. Similarly, C(r+2) = T(TC(r)) = T2 C(r) and in general, C(r+n) = Tn

C(r). Any number can be expressed as a series of some selected powers of two. If all the (T**n) matrices are stored (n = 2**0, 2**1, ..., 2** (k-1)) where (2**k) is the maximum length of the data field), then any power of T can be expressed as a product of one or more of the stored matrices. For a data field with a maximum length of 64K bytes, 16 matrices (T, T2, T4, ..., T32768) are stored. The remainder produced by a byte of data is a function of the input data and the remainder already present (due to previous data having been clocked through the generator). The initial remainder is zero. Since the initial part of the data consists of zero bytes, the state of the remainder is going to remain unchanged, and the initial part may therefore be ignored. Each nonzero byte will, however, produce some change in the remainder. The remainder due to the nonzero bytes, which is the partial CRC, is generated. The zero bytes in the third part now have to be clocked through the generator. Since the initial remainder is nonzero, each zero byte will change the state of the remainder; the zero bytes cannot, therefore, be ignored. However, the remainder at a certain state, R(t), is a function only of the remainder at the previous state, R(t-1). Using the resident processor engine, a typical software implementation of the CRC regeneration procedure outlined above requires (256 x 16) bits of ROM (read-only memory) to store the matrices, and about (40 x 16) bits of program store. If a 16-bit microprocessor with a cycle time of 80 nanoseconds and an average instruction cycle time of 240 nanoseconds is used, updating a 16-bit CRC will take about 0.5 millisecond, assuming (in the worst case) that all 16 matrices are required. In hardware implementation using the processor engine to trigger the operation, a Galois Field Vector Multiplier can be used to multiply two variable input vectors, as shown in Fig. 1. In another hardware approach, the matrix multiplier of Fig. 2 is a direct translation of a typical software technique. Each of the T-matrix multipliers of Fig. 2 (in the second method) will require about 50 two-input gates, resulting in 800 gates. In the GF vector multiplier method of Fig. 1, about 600 two-input gates and (16 x 16) bits of ROM will be required. Assuming a cycle time of 80 nanoseconds, the hardware methods will take (in the worst case) about 20 microseconds to execute.

☐ 12. Document ID: NN86034520

L7: Entry 12 of 19 File: TDBD Mar 1, 1986

TDB-ACC-NO: NN86034520

DISCLOSURE TITLE: Shared Memory Management for Transaction Speed-Up in a Multi-System Environment

L7: Entry 12 of 19 File: TDBD Mar 1, 1986

DOCUMENT-IDENTIFIER: NN86034520
TITLE: Shared Memory Management for Transaction Speed-Up in a Multi-System Environment

Disclosure Title (1):
Shared Memory Management for Transaction Speed-Up in a Multi-System Environment

Disclosure Text (1):
- A method for controlling a shared buffer in a multi-system data-sharing environment that results in significant transaction speedup and reduction in

contention between transactions is described. The decrease in contention allows the multiple systems to sustain a higher transaction throughput. A larger number of systems can be coupled together using this scheme, than without it. In addition, transaction response time is significantly reduced, as described below. The basic system structure assumed here is illustrated in Fig. 1. A number of systems, each running an independent operating system, share a common database. There are two levels of data sharing. All systems have access to a shared memory and to secondary storage (disk). Each system schedules transactions for execution locally. It will be assumed that concurrency control of these transactions is done using locking. This may be through a centralized lock manager or through a distributed lock management scheme they1Ù. The focus here is on data coherency control of the shared memory. That is, all systems must see a consistent version of blocks in the local buffers, shared memory and disk. Current multi-system transaction processing systems do not use the shared memory, and operate essentially as follows they2Ù. (See Fig. 2) In this context, a block is the unit of data transfer between the database disks and the processor's primary memory. A typical block is 4 Kbytes of data. At the end of a transaction, a log is written to non-volatile store (usually disk) and updated blocks are written to shared secondary storage (disk). Following this, broadcast notify messages are sent to all systems in the complex, informing them of blocks that have been modified. Systems receiving this block invalidate message delete these blocks from their local buffers in main memory (Fig. 1) and respond to the requesting system that they have completed their buffer invalidation. If the block is being currently read from shared secondary storage, it will be declared as invalid at the completion of the read. After invalidation completion messages are received from all other systems in the complex, the transaction that did the update can release the lock it had on the updated block. Now any other system that needs this block must read it from secondary storage. Fig. 2 shows the actions for 3 blocks written at the end of the transaction (commit time). (This is the average number of writes per transaction observed in traces analyzed in they1Ù.) Typically, these writes take about 30 milliseconds each, for a total of about 90 milliseconds. During this time all locks are held by the transaction. The shared memory buffer can be used to store updated blocks. (This would be done after writing a log to non-volatile storage for recovery purposes.) Now a transaction that does an update can release locks after writing the block in the shared memory (and after ensuring that data coherency is preserved, as described later). Thus, transaction response time is reduced and locks on a block will be held for a shorter time, leading to lower lock contention. Further, if a contention occurs with an update of the block, the waiting transaction can read the block from shared memory (a few microseconds), rather than from disk (about 30 milliseconds). Finally, the block can be retained in the shared memory with appropriate coherency control. As a result, frequently updated blocks reside in shared memory and frequently read blocks reside in local buffers within the systems, thus making good use of both levels of memory. The method, described here, will be referred to as shared memory block buffering. The basic scheme assuming block only locking is first presented. Following this, extensions to record and block locking, prefetching, non-partitioned shared memory, and speed-up for frequent updates are described. For ease of presentation, the scheme is first described with the following simplifying assumptions. All locks on the database are at the block level, and this is the unit of transfer between disk and buffer storage and between shared memory and buffer storage. The shared memory is partitioned, and each system owns a partition. Only the owning system may write into a partition, while any system may read from all of the shared memory. Reads from disk and shared memory are only done when a read lock is held on the block. Thus, no prefetching of data occurs. These assumptions are relaxed later. It is also assumed that all access to the shared memory and to disk is controlled by a buffer manager function in each system in the complex. This buffer manager manages both the local buffer and the partition of the shared memory owned by the corresponding system. Thus, all requests for (logical) blocks by transactions are through the buffer manager. A mechanism for sending block invalidate messages between systems is also assumed. This may be through a communications medium between systems. Alternatively, the information may be placed in a designated area of shared memory and other systems informed of the message. The actions for the buffer managers are shown in Fig. 3. At the end of the transaction, block changes must be entered in a non-volatile log to enable recovery from a failure. Fig. 3.1 shows the buffer manager actions at transaction commit time after the log write is completed. First, each local buffer block modified by the transaction is updated. The following actions are then performed for each updated block. The buffer manager checks to see if any space is available for the updated block in the shared memory (indicated as SM in Fig. 3) partition of this system. (Recall that the shared memory is partitioned and each partition is managed by each local buffer manager.) If a shared

a previous version is being written to DASD. If another update occurs before the original write completes, the pending write is deleted and the new update's write is set pending. The buffer manager's actions at commit point is shown in Fig. 5.1. The actions are the same as that in Fig. 4.1 except when there is space in SM for the updated blocks and there is an ongoing write to the updated block. If this occurs, the invalidate response from the system that is doing the current write on the block will indicate the ongoing write. The block is now inserted in a write pending queue, to be written out when the current write is completed; the new update is written to DASD when the current write is complete unless still another write to the block occurs in the interim (see below). Locks are released after the entry in the write pending queue is made, and new reads from the block are made from the SM. The actions on receiving an invalidate are shown in Fig. 5.2. The differences from Fig. 3.2 are in the case when the old version of the updated block is in the SM partition of the system receiving the invalidate. If a write on this (old version) block is pending, the pending write is deleted, since it is redundant because of the update. If the block is being written to DASD, it is marked invalid (so that the slot is reclaimed when the write completes) and the response to the invalidate indicates an 'ongoing write' condition. Finally, when the write completion message is received (Fig. 5.3) (as in the record and block lock scheme described above), any pending writes are initiated. Another solution to the frequent update problem is possible if a system can determine that its enqueued write has been initiated and that this write will occur before a subsequent write to the same block from any other system. If this is possible, the response to a block invalidate message can be sent when the write has been initiated, rather than when the write is completed. A further optimization is possible if a previously enqueued block write can be purged (i.e., deleted) if it were not initiated when the block invalidate is received. Fig. 2.1 shows the sequence of events during the course of a transaction in a multi-system data sharing without shared memory (data is shared on the disk only). Locks on updated blocks may be released only after they are written into the disk. In this article, we consider a data-sharing architecture with shared memory. Shared memory may be volatile, and subject to failure. The unit of access of the shared memory is called a slot, and in the basic scheme it is assumed to be the size of a (fixed size) block. (This assumption was relaxed in the extensions discussed in this article.) A technique is discussed that permits the release of locks before the disk writes are complete. As illustrated in Fig. 2.2, in our technique the system writes updated blocks into shared memory, sends the invalidation notification after the shared memory writes are complete, and, when the invalidation responses are received, commits the transaction, releases all locks and initiates the disk writes for the updated blocks from its main memory. One advantage of this scheme is the earlier release of locks (cutting several disk write times from the average lock holding time). This leads to lower lock contentions or allows a higher transaction rate and more systems to be coupled together in a data sharing complex. Further, disk reads due to multi-system buffer invalidation are greatly reduced. Our algorithms, as will be demonstrated in the addendum below, address the following technical issues posed by this modification. At invalidation, an up-to-date copy of the block may not be on disk. They will be required to be obtained from shared memory at least until the disk is updated. Asynchronous disk writes of updated blocks are explicitly serialized in the order of the updates by communicating disk write completion information between systems for the updated blocks. Consistency of data at various levels of the hierarchy is an essential part of this article. Recovery: On the failure of a system - its scheduled disk writes of updated blocks may be lost; however, up-to-date copies of the updated blocks are available in shared memory, and they are copied to disk. On the failure of the shared memory - references to shared memory are directed to the disk for blocks already updated on the disk. For

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☐ 13. Document ID: NB84092655

L7: Entry 13 of 19 File: TDBD Sep 1, 1984

TDB-ACC-NO: NB84092655

DISCLOSURE TITLE: Combined Real/Virtual Fixed-Size Buffer Mechanism in Shared Storage

L7: Entry 13 of 19 File: TDBD Sep 1, 1984

DOCUMENT-IDENTIFIER: NB84092655
TITLE: Combined Real/Virtual Fixed-Size Buffer Mechanism in Shared Storage

Disclosure Title (1):
Combined Real/Virtual Fixed-Size Buffer Mechanism in Shared Storage

Disclosure Text (1):
- The technique to be described provides a combined real/virtual storage mechanism from a common storage pool where a virtual buffer facility uses under-utilized real storage. It can be used with microprocessors with multiple priority interrupt levels where a machine check/program check activates the highest priority interrupt level and where there is no hardware protection to main storage. The control program/operating system of the microprocessor employs machine check/program check error processing on the highest priority interrupt level, an interrupt handler to control level interrupts, device communication on next highest interrupt levels, a control program scheduler and services on next priority interrupt level, and multiple tasking application programs executing basic processor instructions on remaining processor interrupt levels. Volatile control storage is used for system control tables, resident control programs, and as a storage pool into which transient control programs are scatter loaded. Storage is reserved for overlay pages of the control program. Another storage pool provides real fixed size storage blocks to requesting tasks for use as task control blocks, program work areas, and for I/O buffers. Storage allocation for application tasks is a control program service which records allocated storage by task within control tables and available storage within chain entries in a Block Allocation Table (BAT). A system control value is used which defines the maximum number of storage blocks in the storage pool. There is a maximum potential storage demand value for a task which requires to be satisfied before that task can be executed. A task can be rolled out to the direct access storage device (DASD) as it is waiting but not ready for execution at a roll point and another task is ready for execution. A task is executed only if its maximum potential storage demand from roll point to roll point can be made available from the system storage blocks currently available. Tasks often underuse the maximum potential demand made available to the task, when the task is actually being executed. The problem is the ability to satisfy a request for buffer allocation of a buffer combination that is larger than the maximum potential storage demand. It is not possible to increase the maximum potential storage demand because of the limiting effect on the number of concurrent executing tasks. It is then necessary to provide a virtual buffer mechanism in addition to a real buffer mechanism. Frequently there will not be enough storage for an independent virtual buffer mechanism. Existing storage management systems frequently operate at all times with a significant reserve of storage which is unused but which, because of storage management rules, will not be allocated. In the modified storage management subsystem described below, this idle storage is used to implement a cache of virtual storage which is backed by DASD in the form of a magnetic disc store. Each application task is allowed a set of Virtual Buffers each addressed by a Virtual Storage Identifier (VSI) number together with its own application number. The elements of the virtual storage subsystem are a Virtual Storage Dataset, code to access the Virtual Storage Dataset, housekeeping code to support the cache, and data management routines to provide the following virtual storage interface for use by the application task. Assign Virtual Buffer ASSVBUF Get Virtual Buffer (read) GEVBUF Put Virtual Buffer (write) PUTVBUF Release Virtual Buffer RELVBUF The virtual storage cache is composed of storage blocks drawn from the free (i.e., unallocated) storage pool. Blocks used in the cache are placed in a cache storage chain instead of the Freechain and are thus not immediately available to satisfy Getmain requests.

Potential Free Storage value falls below another threshold, modified cache blocks must be written to DASD and thus converted into unmodified blocks. This involves I/O queueing and is not instantaneous, so a higher threshold is required. Housekeeping is also desirable to maintain a reasonable minimum number of CCT entries available for use (i.e., on either the available or the unmodified chain) in order that PSHV requests cause blocks to be accepted into the cache and not have to be released immediately. This is also achieved by writing modified blocks to DASD. (Provided the CCT is of adequate size, blocks are more likely to be written out because of the storage threshold than because of the CCT entries threshold.) If the Potential Free Storage value should fall below the basic storage management system's Free Storage Threshold (which will be lower than its own threshold), then a serious storage underflow exist. This would only occur when writing of modified cache blocks to DASD failed to keep pace with large Getmain requests. This underflow condition will be monitored and a count kept (for problem determination) of the number of times since initial program load that it has occurred. While a cache block is being written to DASD, it is important that it should not be made available from the cache to the application, as (a) it would have to remain flagged as modified, wasting the write, and AB (b) any alteration during the write would affect the DASD read-back check. This is prevented by setting the WRITE-OUT flag in its CCT entry, which also serves to prevent the block being selected for write-out while it is already being written out. Any PULV request for a block so flagged is stacked via a mini-IOCB chained off the CCT header, and is unstacked by the housekeeping function on completion. The STACKED flag is set in the CCT entry to indicate that a PULV request is stacked for the virtual storage block represented by the CCT entry. In determining whether to write a modified cache block to DASD, any such blocks already being written out (as a result of previous housekeeping) are counted towards meeting the threshold, so only the number of writes actually required are initiated. (If this were not done, successive housekeeping passes would continue to initiate writes even if only one was required, until the first write completed.) Only one write can be initiated on each pass through the housekeeping routine, but the routine may be executed many times before a write-out completes, and so it is possible for multiple write-outs to be in progress (i.e., queued for DASD I/O) at the same time. If an I/O error occurs on a housekeeping write to the VSA, the modified block is retained in the cache with the VMAP and WRITE-OUT bits still set, and the I/O error counter in the CCT header is incremented. The system will continue to run with the storage and CCT thresholds apparently reduced, and probably degraded performance. If the error count exceeds the value 2, a system abend (abnormal end) is declared. If a PULV request was stacked for the corresponding area of storage, then the function is resumed but its return code is forced to 'I/O error', so abending the task concerned. The VSA is mapped onto DASD within a System Dataset. Access to the DASD VSA is through Relative Dataset I/O using the Dataset ID and VSA Initial RBN values from the CCT header, which will be initialized during IPL (initial program load). The DSID and initial RBN values used to locate the VSA on DASD are installation dependent and are not assembled into the CCT header. These values are set up as part of system installation. If these details are incomplete, then the system will not operate.

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☐ 14. Document ID: NB84035510

L7: Entry 14 of 19 File: TDBD Mar 1, 1984

TDB-ACC-NO: NB84035510

DISCLOSURE TITLE: System Library Look-Aside Buffer

L7: Entry 14 of 19 File: TDBD Mar 1, 1984

DOCUMENT-IDENTIFIER: NB84035510
TITLE: System Library Look-Aside Buffer

Disclosure Text (1):
- With today's new computers the trend is for CPU speeds to increase at a faster rate than I/O speeds. I/O time is therefore becoming a more significant fraction of each job's time, and the I/O subsystem is being driven nearer to its capacity. This makes it harder for system programmers to tune systems, and I/O bottlenecks are more likely to occur. In addition, today's increasingly powerful computers are permitting more complex workloads with the consequence that system programmers need simpler ways to control the computing systems. Accessing I/O devices to search for and fetch program modules from online system program libraries is a pervasive cause of I/O delays in large systems. As well as tuning the I/O for these libraries, the system programmer needs to control their contents in order to protect system integrity and to provide orderly maintenance. Staging the directories of the online system libraries into a look-aside index residing in CPU-addressable main storage eliminates search I/O and provides a buffer which shields the running system from updates to the libraries. If the look-aside buffer is refreshable, the system programmer can use it as a control point to manage updates to the online system libraries. This reduces I/O accesses to the online system libraries, and make it possible to fetch modules from them at a faster rate. This means that the number or size of the online system libraries can be increased. If adequate integrity checking is added to the module fetch process, it becomes reasonable to allow some unauthorized user libraries to be included in the online system library structure. The end result of using a look-aside buffer in main storage is to increase the responsiveness, capacity, manageability, and utility of the online system libraries. LNKLST Look-aside (LLA) is an example of how such a look-aside buffer was implemented. "LNKLST" (link list) is the term used here to refer to the online system libraries in MVS. LLA improves LNKLST processing in the following ways: (1) LLA provides MVS with a complete in-storage hashed directory for MVS's LNKLST concatenation and a search routine called by MVS's library search service (BLDL). LLA completely eliminates BLDL I/O to the LNKLST directories in a running MVS system. The quality of BLDL search I/O against the LNKLST increases with the size of the system, and it causes severe channel and device contention. (2) LLA's directory is refreshable on operator command. All Updates take effect simultaneously. Switching to the new version is a short process which is serialized with the LLA search routine. This helps installations to control updates to LNKLST data sets. (3) The directory resides in LLA's own private address space (above 16MB virtual and backed above 16MB real). It is thus protected from invalid stores, and it does not intrude on users' addressing ranges. Also, LLA is unlikely to become unduly restricted by other system components because the bulk of LLA's routines are isolated from the rest of them. (4) The LLA directory search routine uses a hashing algorithm, and LLA eliminates the resident BLDL table of LNKLST directory entries. System tuning is simplified because the sequence of LNKLST data sets has no bearing on search time and because all directory entries are obtained without I/O to the directories. Also, frequently used modules whose directory entries would have been in the BLDL table may now be updated without re-IPLing the system. (5) LLA supports a mixture of Authorized Program Facility (APF) and non-APF libraries in the LNKLST via a new system parameter key word. This permits installations to include user libraries in the LNKLST without jeopardizing system integrity. Any APF libraries in the LNKLST continue to be processed as APF libraries. (6) LLA relaxes the 16 data set restriction on the size of the LNKLST concatenation to conform with the standard Data Management limit of over 100 data sets. This provides installations with increased flexibility in building their desired LNKLSTs, and it leaves room for maintenance and expansion. (7) LLA makes limited maintenance of LNKLST data sets possible in a running system because of the buffering effect of the directory (1). Dynamic maintenance is facilitated by the functions in paragraphs (2), (4) and (6) above.

☐ 15. Document ID: NB84035455

L7: Entry 15 of 19 File: TDBD Mar 1, 1984

TDB-ACC-NO: NB84035455

DISCLOSURE TITLE: Adaptive N-Way Associative TABLE Extension Method for Virtual Paging Support

L7: Entry 15 of 19 File: TDBD Mar 1, 1984

DOCUMENT-IDENTIFIER: NB84035455
TITLE: Adaptive N-Way Associative TABLE Extension Method for Virtual Paging Support

Disclosure Text (1):
- Existing virtual memory (VM) paging systems (which typically employ a fixed hash method to access logical-to-physical address translation information from a table) can encounter a severe table miss problem for program processes which accidentally execute an address mix which requires near-simultaneous access of logical address locations that alias to a restricted number of address translation table entries. In some processors (such as the Motorola 68000), this problem can even lead to a closed execution loop if the table is not organized to be sufficiently deep (in terms of number of entries for a particular table address), i.e., sufficiently N-way associative. A chain-pointer-based method can be implemented within the address translation table itself (or in a table external to it) to adaptively make a single level entry address translation table become N-way associative to overcome these potential problems. Figs. 1-2 illustrate two design implementations of a chain-pointer-based method for extending a single level table 1 to N-associative levels in those areas of the table which require it. One of these (Fig. 1) implements an extension table internally within the address translation table 1 itself, and the other (Fig. 2), with an auxiliary fast RAM (random-access memory) table 2 which is attached externally to the address translation table. Both of the designs make use of a chain pointer system 3 to indicate which table entries currently correspond to the logical address equivalence class for a particular translation table address code. In the case of the internal extension design given in Fig. 1, an additional bit tag 4 is also required to distinguish a chained entry from a legitimate local entry for that table address. The basic function of the chain pointer system is to access sequentially a number (possibly N) table entries which are associated with a particular RAM table address. These entries have been loaded under software control via the BIDIRECTIONAL data port 5. When the table is used in the normal address translation mode to access an entry, a COMPARE subunit 6 compares TABLE HASH KEY entry with the current HASH REFERENCE to determine if the entry is associated with the current logical address. A HASH-compare mismatch will cause the chain pointer (if there is one) to be clocked by TABLE MISS into the ADDRESS REG 7 to select the next member in the chain for a similar comparison. Chained entries are, thereby, examined sequentially until a match on HASH characteristic is found or an END chain marker is detected at 9. When END is detected without a HASH match condition, the CONTROL LATCH 8 (which is in the set state until this point) is reset to enable generation of the BERR* active low state to signal table miss to the processor. The above-described process is supported by both implementations (Figs. 1-2). Although it requires more hardware in terms of an extra table, the structure in Fig. 2 also offers the benefit of supporting chained entries without the risk of having entries replaced by an entry which corresponds to that normally selected via the RAM table address input and not the chain pointer. On the other hand, the implementation of Fig. 1 makes more efficient use of the address translation table space than that of Fig. 2, but requires software rearrangement of the chained entries when normal table entries preempt use of the space occupied by a

chained set of entries.

☐ 16. Document ID: NN80081190

L7: Entry 16 of 19 File: TDBD Aug 1, 1980

TDB-ACC-NO: NN80081190

DISCLOSURE TITLE: Electronically Changeable Keyboard Key Inscriptions. August 1980.

L7: Entry 16 of 19 File: TDBD Aug 1, 1980

DOCUMENT-IDENTIFIER: NN80081190
TITLE: Electronically Changeable Keyboard Key Inscriptions. August 1980.

Disclosure Title (1):
Electronically Changeable Keyboard Key Inscriptions. August 1980.

Disclosure Text (1):
4p. This invention relates to a keyboard having electronically alterable inscriptions obtained through the use in each key of an associated dot matrix drive logic, which logic excites a counterpart key top electronic display. The matrix of keys are coupled to a random-access memory of diverse symbols accessible for altering the keys during a predetermined portion of a recurrent cycle. - In this keyboard, multiple inscriptions are replaced by an electronic display. The symbol displayed is programmable, and each key displays whatever it was told to display during the programming phase. Once programmed, each key displays the symbol which the system understands to be the meaning of that key. If the character set of the keyboard is changed, the keyboard is caused to display the new symbols by going through the programming phase again. - The logic chip of Fig. 1 has the 84 bits stored, and has the drivers for the LED (light-emitting diode) or LCD (liquid crystal display) display. It can have an internal oscillator, but we will assume that a global clock signal is broadcast to each key. Each key uses the clock to cycle through the rows and columns of the LED device, continually blinking the symbol. This is state of the art technology for digital watches, and will not be described here. What remains is to describe the key programming phase during which each key receives the 84 bits which define the symbol to be displayed. To do this, we provide each key with a unique data line. The data line is used during the programming phase to transmit to each key a sequence of 84 bits. We now describe the action of the keyboard controller to do this. This is done with the aid of Figs. 2, 3 and 4. - Fig. 2 shows a conceptual keyboard configuration with 64 keys. (The method does not depend on how the keys are arranged or how many there are. We simply number them 0 through (n-1), if there are "n" keys.) Each key has two logic signal inputs, DATA signal inputs and KEY CLOCK. Fig. 3 is a block diagram of that portion of the keyboard controller charged with the key programming phase function. The Data Register is 64 bits wide and has one bit line for each key. This is the unique Data input wire for each key. An address counter reads out successive words from the random-access memory table, in synchronism with the KEY CLOCK, the clock line which feeds each key, as shown in Fig. 2. The high-order address bits ADR10-2 are preset; they indicate which of 8 symbol sets are to be programmed. The timing chart for the key programming phase is shown in Fig. 4. When a decision is made to change the symbols, the high-order 3 address bits of ADR can be loaded and the low-order bit

counter can be cleared to 0, via control signal INITPROG. Following an access time propagation delay, the first symbol bit (BIT or pel 0) for each of the 64 keys appears on the random-access memory 64 bit wide bus out. - The key programming phase is initiated by the clearing of ADR (3-9). This allows the READ-OUT CLOCK to advance the counter and clock random-access memory data out into the DATA Register. An important technique for notifying the keys that the key programming phase is to begin is identified by time t1 in Fig. 4. This is the only time the Data line makes a 0-1 transition when signal KEY CLOCK is high. This can be detected by a simple circuit, as shown in Fig. 5. It "resets" the individual Key logic, and prepares the chip to receive the 84-bit symbol. The 0-1 transition on each Data line is generated, as shown, by AND 1, and 64 OR gates 2. Note READOUT CLK leads KEY CLOCK, by 90 in phase. - The next occurrence of KEY CLOCK, denoted time t2 in Fig. 4, the first symbol bit is valid on each Data line. On the following KEY CLOCK, the second symbol bits are valid on the Data line. - This goes on until 84 cycles and 84 data bits have been sent to each key. A decode AND gate 3 detects the 85th period since the start, and clears the Data Register and clocks the advance of the 7-bit address counter ADR (3-9), thus ending the key programming phase. - The logic at the key for the key programming phase is shown in Fig. 5. The 84-bit random-access memory stores the symbol. The 0-1 transition on Data when KEY CLOCK is valid is detected by flip-flop 1, activating signal INIT which clears CTR 20. At the fall of KEY CLOCK, INIT sets PROG flip-flop 3. PROG clears INIT. NAND 4 generates an active-low Write Enable signal for the random-access memory at the next activation of KEY CLOCK. DATA is valid with the first symbol bit or pel at this time. When KEY CLOCK deactivates, the DATA is written in random-access memory address 0, and CTR is advanced to address 1. At the next KEY CLOCK activation, the second symbol pel is valid on DATA. This pel bit value is similarly written to random-access memory. These cycles continue until the counter is advanced to 84. Detection circuit 5 is activated and clears PROG, ending the key programming phase.

☐ 17. Document ID: NN8006379

L7: Entry 17 of 19 File: TDBD Jun 1, 1980

TDB-ACC-NO: NN8006379

DISCLOSURE TITLE: Integrated Bipolar-FET Static Memory Cell. June 1980.

L7: Entry 17 of 19 File: TDBD Jun 1, 1980

DOCUMENT-IDENTIFIER: NN8006379
TITLE: Integrated Bipolar-FET Static Memory Cell. June 1980.

Disclosure Text (1):
2p. A static random-access memory is described with approximately the same silicon chip area occupied by a comparable dynamic random-access memory. - A single bipolar transistor shown in Fig. 1 (either pnp as shown in Fig. 1A or npn as shown in Fig. 1B) can exhibit two stable states when the collector-base voltage is large enough to cause avalanche multiplication. The "OFF" state occurs when both the base and emitter are grounded and the collector is at V(cc). No carriers are injected from the emitter, and the only current is leakage from the reverse biased collector base junction. This current leaks to ground through R(B), raising the base potential a few mV but not enough to cause injection from the emitter. The "ON" state is

characterized by a forward biased base-emitter junction. Carriers are injected from the emitter, traverse the base, and are collected. The collection field is sufficient to cause avalanche multiplication, creating a flow of holes in an npn transistor or electrons in a pnp transistor into the base. These supply the charge necessary to keep the emitter-base junction forward biased. The avalanche-created carriers provide the current that passes through R(B) the carriers that are lost by recombination in the base, and those that are injected into the emitter. - The mechanism described above has been proposed by W. Tantraporn et al, in IEEE Trans. on Electron Devices, May 1978, in a paper entitled, "Si-Controlled Avalanche Logic". The authors discuss the use of controlled avalanche regions to increase the speed of Si devices and describe the operation of an avalanche memory triode using small resistor values of about 1000 ohms to gain speed. - Static memory operation has been obtained for the circuits shown in Figs. 1A and 1B, with R(B) from 22 mega-ohms to 100 kilo-ohms and R(E) from 1 M-ohm to 20 K-ohm. The V(CC) of the transistor may be on the order of 25 V. A low is written if V(IN) is 0 volt and the base switch is momentarily closed, and the transistor switches to the "OFF" state. A high is written if V(IN) is greater than 0.7 V and the base switch is momentarily closed. Upon opening the base switch, the positive feedback provided by avalanche multiplication causes the emitter current to increase. This causes V(E) and V(B) to rise, while maintaining the junction's forward bias. As V(B) increases, more current leaks out of R(B) and the avalanche multiplication decreases. These factors cause the emitter current to stabilize when V(CB) has dropped by several volts. - As shown in Fig. 2, for MOSFETs as switches and as bipolar transistor, a nondestructive read can be obtained by connecting V(IN) to ground through an impedance on the order of R(B), and then closing the base switch. A voltage greater than 0.7 V indicates "ON", and 0 V indicates "OFF". - It is noted in the IEEE article by Tantraporn et al that an avalanche memory triode can be used as a memory cell with matrix addressing. This approach required perpendicular layers of metallization. Another technology which is illustrated by Fig. 3 is to replace the capacitor in a known dynamic random-access memory design by a bipolar transistor operating as an avalanche memory triode. The memory operation is unchanged. With the substrate negative, grounding the word line permits conduction between the source and drain. The potential on the bit line is written into the chosen device. To read, the bit line is floated, and the voltage impressed on it by the chosen device is sensed.

☐ 18. Document ID: NB78045060

L7: Entry 18 of 19 File: TDBD Apr 1, 1978

TDB-ACC-NO: NB78045060

DISCLOSURE TITLE: Structure of Performance Monitor for Distributed Computer Systems. April 1978.

L7: Entry 18 of 19 File: TDBD Apr 1, 1978

DOCUMENT-IDENTIFIER: NB78045060
TITLE: Structure of Performance Monitor for Distributed Computer Systems. April 1978.

Disclosure Text (1):
6p. This article describes a generalized design of a Performance Monitor for

☐ 19. Document ID: NN77122839

L7: Entry 19 of 19 File: TDBD Dec 1, 1977

TDB-ACC-NO: NN77122839

DISCLOSURE TITLE: Josephson Memory Cell With Magnetic Film. December 1977.

L7: Entry 19 of 19 File: TDBD Dec 1, 1977

DOCUMENT-IDENTIFIER: NN77122839
TITLE: Josephson Memory Cell With Magnetic Film. December 1977.

Disclosure Text (1):
2p. Thin magnetic films are combined with Josephson devices. In a logic gate or in a memory cell a Josephson junction is provided with a thin magnetic film. The easy axis extends in the film plane parallel to the junction width dimension. The film, e.g., permalloy, shows a substantially rectangular hysteresis loop. - By proper switching of the film's magnetization it can be utilized to bias the Josephson junction magnetically or to write-in the cell, respectively. In addition, the control lines for switching the Josephson junction can be used to switch the film magnetically. The coercive field of the magnetic film can be controlled to ensure that it switches at fields of greater magnitude than those normally required to switch the Josephson junction. An example shows a read-mostly memory. Readout with switching the Josephson junction is very fast, and the relatively slow magnetization change for writing has to occur only occasionally. - Depicted is a cross-section of a memory cell. On a gate string G the overlapping ends of alternating M2-M3 metallic strips comprise therebetween the thin oxide layer defining a Josephson junction. The superconducting ground-plane (M1) with its covering insulation layer is not shown for clarity. Two narrow control lines cross the junction area in parallel transverse to the gate line G and insulated therefrom. These X, Y lines are the coordinate access lines of the memory array. To permit parallelism in the junction area, the Y line has to be meandered in the memory matrix. A thin magnetic film is arranged on top of the crossing points and insulated from them. - Provided the magnetic film is not driven into saturation, the gate current (I-G) dependence on control current (I-C) is similar to that of a junction without film, as shown by the symmetric characteristic in solid lines. At increasing I-C the magnetic film will reach saturation at a certain value I-CO. At currents above I-CO the film magnetization remains constant. The characteristic is changed to a curve that may be assigned the binary value "1". Reducing the control current, the gate current follows this curve until a sign change of film magnetization occurs where the control current crosses value -I-CO in the negative. Then the characteristic is changed to another curve branch that may be assigned the other binary value "0". Depending on film magnetization the Josephson junction shows different switching behavior characterized by the two distinct branches of the characteristic. - For writing, the X line and the Y line are used according to the coincidence principle to access a selected cell with a net control current exceeding the value I-CO (or -I-CO) to set the respective film magnetization. For read-out, current is applied first to the appropriate X control line, followed by a pulse on the selected gate string. Detection of a "0" or "1" is determined by the presence or absence of a voltage on the gate string G.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw. Desc | Clip Img

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Set     Items   Descripti
S1        379   AU=(NAKAMURA L? OR NAKAMURA, L? OR TATE S? OR TATE, S?)
S2         27   S1 AND IC=G06F?
S3         27   IDPAT (sorted in duplicate/non-duplicate order)
S4         25   IDPAT (primary/non-duplicate records only)
File 344:Chinese Patents Abs Aug 1985-2002/Sep
         (c) 2002 European Patent Office
File 347:JAPIO Oct 1976-2002/May(Updated 020903)
         (c) 2002 JPO & JAPIO
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200261
         (c) 2002  Thomson Derwent
File 348:EUROPEAN PATENTS 1978-2002/Sep W03
         (c) 2002 European Patent Office
File 349:PCT FULLTEXT 1983-2002/UB=20020912,UT=20020905
         (c) 2002 WIPO/Univentio
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4/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014398377 **Image available**
WPI Acc No: 2002-219080/200228
XRPX Acc No: N02-168080
Presenting data in limited display area of web page, involves displaying graphical element in one portion of screen indicating that there is another portion of data within display area
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: **NAKAMURA L E**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2360431	A	20010919	GB 200031243	A	20001221	200228	B

Priority Applications (No Type Date): US 2000478974 A 20000106
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2360431	A		19	G06F-003/033	

Abstract (Basic): GB 2360431 A
NOVELTY - A page is displayed on one portion of the display area and a graphical element is displayed indicating that there is another portion of data within the display area. The two portions of the data are selectively enabled in response to user input.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:
(1) A data presenting system for output to computer display.
(2) A computer program for outputting data to a computer display.
USE - For presenting data in limited display area of web pages such as hyper text markup language (HTML) page, dynamic hyper text markup language (DHTML) page, extensible markup language (XML) page, standard generalized markup language (SGML) page, etc.
ADVANTAGE - As graphical element is displayed on a portion of the screen, lengthy fields are displayed as graphical element so that user can effectively choose any portion of display screen.
DESCRIPTION OF DRAWING(S) - The figure shows the display of database records in HTML page.
pp; 19 DwgNo 3/4
Title Terms: PRESENT; DATA; LIMIT; DISPLAY; AREA; WEB; PAGE; DISPLAY; GRAPHICAL; ELEMENT; ONE; PORTION; SCREEN; INDICATE; PORTION; DATA; DISPLAY; AREA
Derwent Class: T01
International Patent Class (Main): **G06F-003/033**
File Segment: EPI

4/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014050896 **Image available**
WPI Acc No: 2001-535109/200159
Related WPI Acc No: 2001-146373
XRPX Acc No: N01-397275
Web page information presentation method involves presenting selectable item list information and selected item information simultaneously on same web page with uniform background
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: **NAKAMURA L E ; TATE S E**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6275833	B1	20010814	US 97892842	A	19970711	200159	B
			US 2000480000	A	20000110		

Priority Applications (No Type Date): US 97892842 A 19970711; US 2000480000

A 20000110

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6275833	B1		14	G06F-017/30	Div ex application US 97892842 Div ex patent US 6178433

Abstract (Basic): US 6275833 B1

NOVELTY - A world wide web (WWW) page is dynamically generated in response to request for presentation of information. The information indicating a list of selectable items is displayed in one area of the WWW page. Another information generated for selected item is simultaneously displayed in other area of the same page without a change in color of background (80).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for web page information presentation system.

USE - For presentation of web page information.

ADVANTAGE - Due to presentation of both selectable item list and selected item information simultaneously on same web page in different presentation areas, information from same/different files can be displayed at the same time without requiring a frame capable web browser. Hence a single, unified background image is presented by the web browser. As there is no need for frame capable web browser, difficulties in managing and maintaining redundant information, are eliminated.

DESCRIPTION OF DRAWING(S) - The figure shows several presentation areas with uniform background.

Background (80)

pp; 14 DwgNo 8/8

Title Terms: WEB; PAGE; INFORMATION; PRESENT; METHOD; PRESENT; SELECT; ITEM ; LIST; INFORMATION; SELECT; ITEM; INFORMATION; SIMULTANEOUS; WEB; PAGE; UNIFORM; BACKGROUND

Derwent Class: T01

International Patent Class (Main): **G06F-017/30**

File Segment: EPI

4/5/3 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013662161 **Image available**

WPI Acc No: 2001-146373/200115

Related WPI Acc No: 1999-394084; 2001-535341

XRPX Acc No: N01-107106

Information presentation method for web pages using dynamic page builder to generate and manage contents on web site

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)

Inventor: **NAKAMURA L E ; TATE S E**

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6178433	B1	20010123	US 97892842	A	19970715	200115	B

Priority Applications (No Type Date): US 97892842 A 19970715

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6178433	B1		14	G06F-017/30	

Abstract (Basic): US 6178433 B1

NOVELTY - The web browser is controlled by the web macro and web server to make the presentation appear with borders around various logical frames. The HTML generated based on the macro causes the browser to create a pseudo-border so that presentation materials can be generated based on selection of the items in a previously presented material.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a system for using a dynamic presentation page builder.

USE - For web pages.

ADVANTAGE - A single unified background image can be presented by a web-browser that presents frames of information. hence, allowing ease of administration while presenting to a user portion of files requested for maximum performance.

DESCRIPTION OF DRAWING(S) - The figure shows display of materials with pseudo-frames.

pp; 14 DwgNo 7/8

Title Terms: INFORMATION; PRESENT; METHOD; WEB; PAGE; DYNAMIC; PAGE; BUILD; GENERATE; MANAGE; CONTENT; WEB; SITE

Derwent Class: T01

International Patent Class (Main): **G06F-017/30**

File Segment: EPI

4/5/4 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

011021304 **Image available**

WPI Acc No: 1996-518254/199651

XRPX Acc No: N96-436768

Time division multiple access processing system for distributed processing system - has function circuit card assemblies that performs series or parallel function operations on information passed from one function circuit card assembly unidirectionally to downstream function circuit card assembly

Patent Assignee: UNISYS CORP (BURS)

Inventor: GRIFFIN D M; LINDSAY R A; SAWYER L D; **TATE S C**

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5574951	A	19961112	US 9332576	A	19930317	199651	B

Priority Applications (No Type Date): US 9332576 A 19930317

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5574951	A		14	G06F-013/00	

Abstract (Basic): US 5574951 A

The system includes a number of parallel lines on the bus structure interconnecting the output pins on one receptacle with the input pins on an adjacent receptacle. Function circuit card assemblies connected to the receptacles of the bus structure to form a daisy chain for performing logic functions on the data. Each circuit card assembly has a plug connection for connecting its input and output pins to the receptacles to form the daisy chain. A source circuit card assembly coupled to a source of high speed data for supplies the high speed data information with destination addresses onto the bus structure. A destination circuit card assembly removes the information from the bus structure. The function circuit card assemblies performs series or parallel function operations on information passed from one function circuit card assembly unidirectionally to a downstream function circuit card assembly to provide a time division random access data processing system.

ADVANTAGE - Provides time division multiple access bus system that eliminates waste of time slots. Provides highly flexible modular bus system that permits change circuit card assemblies position without change in protocol or software.

Dwg.3a,/6

Title Terms: TIME; DIVIDE; MULTIPLE; ACCESS; PROCESS; SYSTEM; DISTRIBUTE; PROCESS; SYSTEM; FUNCTION; CIRCUIT; CARD; ASSEMBLE; PERFORMANCE; SERIES; PARALLEL; FUNCTION; OPERATE; INFORMATION; PASS; ONE; FUNCTION; CIRCUIT; CARD; ASSEMBLE; UNIDIRECTIONAL; DOWNSTREAM; FUNCTION; CIRCUIT; CARD; ASSEMBLE

Derwent Class: T01

International Patent Class (Main): **G06F-013/00**

International Patent Class (Additional): **G06F-013/20**

File Segment: EPI

4/5/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010260160 **Image available**
WPI Acc No: 1995-161415/199521
XRPX Acc No: N95-126656
Interface unit circuit with on-chip test simulation - has input simulation points for testing interface gate array chip in real-time or step-by-step mode
Patent Assignee: UNISYS CORP (BURS)
Inventor: EVANS L A; GODDERIDGE D R; **TATE S C**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5408631	A	19950418	US 9332575	A	19930317	199521	B

Priority Applications (No Type Date): US 9332575 A 19930317
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5408631	A		13	G06F-013/00	

Abstract (Basic): US 5408631 A
The interface unit circuit for connecting circuit card assemblies to a data stream and to each other is designed for implementation on a high speed semiconductor chip. A parallel bit data word comprising a programmable address field is compared to a mask address stored in buffer registers and in the presence of a match, and the parallel bit data word is stored in a sink register.
The address field of the data word is filled with zeros and passed to the output of the data channel where the time slot for the data word may be written over with new data words or the time slot passed on to other circuit card assemblies or other elements.
USE/ADVANTAGE - Low logic level interface circuit for use on circuit card assemblies and implementation on single gallium arsenide chip. Compatible with ECL functional elements operating at 200 mega-words per second. Accepts software test programs for testing interface circuit.
Dwg.1/7
Title Terms: INTERFACE; UNIT; CIRCUIT; CHIP; TEST; SIMULATE; INPUT; SIMULATE; POINT; TEST; INTERFACE; GATE; ARRAY; CHIP; REAL; TIME; STEP; STEP; MODE
Derwent Class: T01
International Patent Class (Main): **G06F-013/00**
File Segment: EPI

4/5/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010121828 **Image available**
WPI Acc No: 1995-023079/199503
XRPX Acc No: N95-017876
Remote alteration method for token value stored in smart card - using local private terminal to establish link between card and remote terminal for passing secure authentication and transaction messages
Patent Assignee: VERIFONE INC (VERI-N); HEWLETT-PACKARD CO (HEWP)
Inventor: **NAKAMURA L S** ; ROBERTS A B; SHEETS J F
Number of Countries: 054 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9428498	A1	19941208	WO 94US6031	A	19940602	199503	B
AU 9469600	A	19941220	AU 9469600	A	19940602	199512	
			WO 94US6031	A	19940602		
EP 701718	A1	19960320	EP 94918158	A	19940602	199616	

			WO 94US6031	A	19940602	
JP 9500743	W	19970121	WO 94US6031	A	19940602	199713
			JP 95500997	A	19940602	
AU 675550	B	19970206	AU 9469600	A	19940602	199714
CN 1127045	A	19960717	CN 94192780	A	19940602	199749
US 5917168	A	19990629	US 9371283	A	19930602	199932
			WO 94US6031	A	19940602	
			US 96578718	A	19960418	
BR 9406733	A	20000425	BR 946733	A	19940602	200033
			WO 94US6031	A	19940602	

Priority Applications (No Type Date): US 9371283 A 19930602; US 96578718 A 19960418
Cited Patents: US 4625276; US 4634845; US 4736094; US 4839504; US 4988849; US 5025373
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9428498	A1	E	38	G06F-015/30	
Designated States (National): AT AU BB BG BR BY CA CH CN CZ DE DK ES FI GB GE HU JP KG KP KR KZ LK LU LV MD MG MN MW NL NO NZ PL PT RO RU SD SE SI SK TJ TT UA US UZ VN					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL OA PT SE					
AU 9469600	A			G06F-015/30	Based on patent WO 9428498
EP 701718	A1	E	38	G06F-015/30	Based on patent WO 9428498
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LI LU MC NL PT SE					
JP 9500743	W		40	G06F-019/00	Based on patent WO 9428498
AU 675550	B			G06F-015/30	Previous Publ. patent AU 9469600
					Based on patent WO 9428498
CN 1127045	A			G06F-017/60	
US 5917168	A			G06F-015/30	CIP of application US 9371283
					Based on patent WO 9428498
BR 9406733	A			G06F-017/60	Based on patent WO 9428498

Abstract (Basic): WO 9428498 A

The method involves establishing a card data link to a data communication interface in the smart card. A card holder data security message is communicated to the card via the link to enable card security programs to produce secure card holder identification data.

A data link to an operatively compatible terminal at a remote location is established and secure transaction messages are communicated between the card and the terminal via the card data link and terminal data link. The messages include token change vector data from the card holder to enable the card and the terminal to perform mutual authentication functions and execute a secure token value change transaction.

ADVANTAGE - Allows use of simple, low cost private terminal, which is not dedicated to particular card holder, since card and remote terminal compare all secure messages and handle programmed transaction activity. Reduces risk of fraud, since private terminal is incapable of interacting with card for transaction activities.

Dwg.3/8

Title Terms: REMOTE; ALTER; METHOD; TOKEN; VALUE; STORAGE; SMART; CARD; LOCAL; PRIVATE; TERMINAL; ESTABLISH; LINK; CARD; REMOTE; TERMINAL; PASS; SECURE; AUTHENTICITY; TRANSACTION; MESSAGE
Derwent Class: T01; T04; T05; W01
International Patent Class (Main): **G06F-015/30 ; G06F-017/60 ; G06F-019/00**
International Patent Class (Additional): G06T-001/00
File Segment: EPI

4/5/7 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

07264501 **Image available**

MEDICAL TREATMENT INFOR[redacted]TION SYSTEM IN HOSPITAL FOR[redacted]EVENTING FALSE RECOGNITION OF PATIENT

PUB. NO.: 2002-132962 [JP 2002132962 A]
PUBLISHED: May 10, 2002 (20020510)
INVENTOR(s): KONDO YOSHIAKI
TATE SHINRI
APPLICANT(s): KONDO YOSHIAKI
TATE SHINRI
NAGASE & CO LTD
APPL. NO.: 2000-369302 [JP 2000369302]
FILED: October 27, 2000 (20001027)
INTL CLASS: **G06F-017/60** ; A61B-005/00; A61J-001/14; A61J-003/00

ABSTRACT

PROBLEM TO BE SOLVED: To avoid taking risks by sorting and processing even a small mistakes in real-time, in an accident that frequently takes place at a medical on site.
SOLUTION: A hub using a twist pain cable is used as a terminal, and a PDA as a portable information terminal for hospital is arranged in each room in a wireless LAN, which is connected respectively or independently to information access servers other than a department in charge in the hospital and makes a part of a trunk LAN wireless, processing is conducted in real time, patient information is written by a bar code or non-contact RF-ID, a wristband put on the patient, where a facial photograph is printed and read, information stored in the server is fetched, data and the facial photograph are displayed on a display, the patient himself is also confirmed as the person in question by roll call by reading out, and people around the patient are made to recognize and confirm the patient at the same time.

4/5/8 (Item 8 from file: 347)

06427501 **Image available**
ATTACHMENT DEVICES AND ELECTRONIC APPARATUS

PUB. NO.: 2000-013064 [JP 2000013064 A]
PUBLISHED: January 14, 2000 (20000114)
INVENTOR(s): MIYAHARA MASAHARU
TATE SUMIO
SUGIMOTO KAZUHIKO
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD
APPL. NO.: 10-176871 [JP 98176871]
FILED: June 24, 1998 (19980624)
INTL CLASS: H05K-007/20; F25D-001/00; **G06F-001/18** ; **G06F-001/20**

ABSTRACT

PROBLEM TO BE SOLVED: To enable realizing attachment devices where discharging efficiency of heat is excellent, and heat radiation control is easy, and realizing miniaturization, thinning, improvement of productivity, multifunction and high performance.

SOLUTION: Thermal connectors 3a, 4a are arranged on attachment devices 3, 4 and connected with heat conducting members 19, 20, which are connected with cooling equipment 18. Heat generated in the attachment devices 3, 4 is introduced to the cooling equipment 18 via the thermal connectors 3a, 4a and the heat conducting members 19, 20, and heat dissipation is effectively performed.

4/5/9 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

06364137 **Image available**
INTERACTIVE VISUAL PRESENTATION DEVICE

PUB. NO.: 11-305747 [JP 11305747 A]
PUBLISHED: November 05, 1999 (19991105)
INVENTOR(s): INAMI MASAHIKO
KAWAKAMI NAOKI
YANAGIDA YASUYUKI
MAEDA TARO
TATE SUSUMU
APPLICANT(s): INAMI MASAHIKO
KAWAKAMI NAOKI
YANAGIDA YASUYUKI
MAEDA TARO
TACHI SUSUMU
APPL. NO.: 10-153542 [JP 98153542]
FILED: April 23, 1998 (19980423)
INTL CLASS: G09G-005/00; A63F-009/22; **G06F-003/00**

ABSTRACT
PROBLEM TO BE SOLVED: To actualize the visual presentation device which is smallsized, lightweight, and portable and to give image presentation corresponding to operation on the device.

SOLUTION: A display 1 is fitted with a tilt, speed, and acceleration sensor 2. The tilt, speed, and acceleration sensor 2 and a control part 4 measure and calculate the attitude and position of the display 1 and the attitude of an observer 3 and a graphic engine part 5 generates an image corresponding to the attitude and position of the liquid crystal display 1 and the visual point of the observer 3.

4/5/10 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

05893819 **Image available**
SHAPE-INPUTTING DEVICE

PUB. NO.: 10-176919 [JP 10176919 A]
PUBLISHED: June 30, 1998 (19980630)
INVENTOR(s): ARAI KAZUHIKO
TATE SUSUMU
APPLICANT(s): OLYMPUS OPTICAL CO LTD [000037] (A Japanese Company or Corporation), JP (Japan)
TATE SUSUMU [000000] (An Individual), JP (Japan)
APPL. NO.: 08-338529 [JP 96338529]
FILED: December 18, 1996 (19961218)
INTL CLASS: [6] G01B-021/22; G01B-007/28; **G06F-003/033**
JAPIO CLASS: 46.1 (INSTRUMENTATION -- Measurement); 45.3 (INFORMATION PROCESSING -- Input Output Units)

ABSTRACT
PROBLEM TO BE SOLVED: To provide a shape-inputting device for inputting the shape change of an object accurately and easily.

SOLUTION: This device has a shape-inputting assembly 2 that is extended from a wrist 2 to a finger tip 10 so that the shape change in a hand 4 can be detected, and the shape-inputting assembly 2 has first to fourth amount-of- stretch detection units 8a, 8b, and 8c for separately detecting the amount of stretch between joints while being arranged between the

joints of the hand, a amount-of-flex detection uni for separating detecting the amount of flex of each joint of the hand, and a connection means 38 for combining the amount- of-stretch detection unit and the amount-of-flex detection unit corresponding to the dimension and shape of the hand.

4/5/11 (Item 11 from file: 347)

05678154 **Image available**
METHOD FOR DEFINING CONSTITUTION OF DISK ARRAY SUB-SYSTEM

PUB. NO.: 09-292954 [JP 9292954 A]
PUBLISHED: November 11, 1997 (19971111)
INVENTOR(s): NAKAMURA HIROYUKI
NABEKURA SUKETAKA
SHINDO TAKEFUMI
TATE SHIGEKI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
HITACHI MICROCOMPUT SYST LTD [470864] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-106814 [JP 96106814]
FILED: April 26, 1996 (19960426)
INTL CLASS: [6] **G06F-003/06**
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units)

ABSTRACT

PROBLEM TO BE SOLVED: To arbitrarily and easily increase, decrease data and change the setting with a logic group as unit by selecting a logic unit for defining the constitution and inputting constitution definition data with a screen operation.

SOLUTION: The disk array sub-system 1 has a disk controller(DKC) 11, disk devices(DKU) 12-a to 12-d and a service processor(SVP) 13. Software 13.1 operating in SVP 13 is provided with a constitution setting function 13.11 having a constitution setting part 13.11.1 and a constitution transmission part 13.11.2, with a maintenance function 13.13. and with a communication function 13.14. In the constitution setting part 13.11.1, setting is inputted and it is outputted to a file as constitution definition data 13.12. The constitution definition data 13.12 is transmitted to the disk controller 11 through the communication function 13.14 by the constitution transmission part 13.11.2 and the disk controller 1 sets the constitution of the device.

4/5/12 (Item 12 from file: 347)

04712349 **Image available**
TRAIN OPERATION CONTROL DEVICE

PUB. NO.: 06-183349 [JP 6183349 A]
PUBLISHED: July 05, 1994 (19940705)
INVENTOR(s): **TATE SEISAKU**
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-338614 [JP 92338614]
FILED: December 18, 1992 (19921218)
INTL CLASS: [5] B61L-027/00; **G06F-015/21**
JAPIO CLASS: 44.9 (COMMUNICATION -- Other); 26.1 (TRANSPORTATION -- Railways); 45.4 (INFORMATION PROCESSING -- Computer Applications)

ABSTRACT

PURPOSE: To provide a [redacted]ain operation control devic[redacted]low-priced and excellent in responsiveness by making not only the operation control device but also each terminal device have a diagram file so that each terminal device receives the input of information and checks the input at the operation arranging time.

CONSTITUTION: When operation arrangement information such as the change of a diagram is inputted. into a terminal device 14a, for instance, the terminal device 14a checks the input of the operation arrangement information and performs transmission to an operation control device 13 when the checked result has no problem. The operation control device 13 checks the state among trains using a control diagram and an operation state file on the basis of this operation arrangement information, and in the case of no problem, instruct the respective terminal devices 14a, 14b, 14c to correct the diagram. The instruction of correction is performed using broadcasting (simultaneous communication) function in a bus-type LAN 15. After the instruction of correction, the operation control device 13 corrects the control diagram in a data file.

4/5/13 (Item 13 from file: 347)

04676570 **Image available**
ACCESS MANAGEMENT SYSTEM

PUB. NO.: 06-348470 [JP 6348470 A]
PUBLISHED: December 22, 1994 (19941222)
INVENTOR(s): YUASA YASUSHI
SAKAMOTO KAZUHIKO
HONMA KAZUHIRO
TATE SHIGEKI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
HITACHI KEIYO ENG CO LTD [485526] (A Japanese Company or Corporation), JP (Japan)
HITACHI MICOM SYST KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-138157 [JP 93138157]
FILED: June 10, 1993 (19930610)
INTL CLASS: [5] **G06F-009/06 ; G06F-012/00**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.2 (INFORMATION PROCESSING -- Memory Units)

ABSTRACT

PURPOSE: To efficiently access a product related to the utilization of a product to be prepared for every process in software development.

CONSTITUTION: A file system for automatically changing the access right of software products previously existing among plural computers connected through plural networks for executing software developing work in each work of software development including at least one software developer is provided with a step (a) for requiring a change in the access right of a product prepared by another developer from a certain developer participating in the software development. a step (b) for sending the content of the request to a product owner having prepared the requested product, a step (c) for enabling the products owner to judge the request based upon the sent request contents, a step (d) for enabling the product owner to execute access right changing processing matched with the judged contents, and a step (e) for informing the developer to whom the access right changing request is sent of the contents of the execution.

4/5/14 (Item 14 from file: 347)

04559050 **Image available**

TASK CONTROL METHOD IN D[redacted]NTRALIZED PROCESSING ENVIRONME[redacted]

PUB. NO.: 06-230950 [JP 6230950 A]
PUBLISHED: August 19, 1994 (19940819)
INVENTOR(s): YUASA YASUSHI
SAKAMOTO KAZUHIKO
HONMA KAZUHIRO
TATE SHIGEKI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
HITACHI KEIYO ENG CO LTD [485526] (A Japanese Company or Corporation), JP (Japan)
HITACHI MICOM SYST KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-013198 [JP 9313198]
FILED: January 29, 1993 (19930129)
INTL CLASS: [5] **G06F-009/06 ; G06F-015/21**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.4 (INFORMATION PROCESSING -- Computer Applications)
JOURNAL: Section: P, Section No. 1830, Vol. 18, No. 614, Pg. 65, November 22, 1994 (19941122)

ABSTRACT

PURPOSE: To support a person who has the delay in development of software.

CONSTITUTION: Four steps are set among plural computers which are connected together via plural networks for development of software. That is, the progress state of working is extracted as the result information in a step (a) for each person working for development of software, the development plan information is extracted out of a storage where the software development plan is previously registered in a step (b), the contents of extracted information are compared with each other in a step (c), and the value showing the priority are sutomatically decided to all processings that are performed by the developer persons through computers in a step (d). In such a process of software development, the progress state of working of each person is compared with the development plan defined previously and the priority value is automatically decided to each processing. Thus the working efficiency is improved for development of software.

4/5/15 (Item 15 from file: 347)

04480369 **Image available**
DATA MANAGING METHOD FOR DISTRIBUTED PROCESSING SYSTEM

PUB. NO.: 06-124269 [JP 6124269 A]
PUBLISHED: May 06, 1994 (19940506)
INVENTOR(s): IKEUCHI YOSHIMA
SAKAMOTO KAZUHIKO
HONMA KAZUHIRO
TATE SHIGEKI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
HITACHI MICOM SYST KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-274756 [JP 92274756]
FILED: October 14, 1992 (19921014)
INTL CLASS: [5] **G06F-015/16**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications)
JOURNAL: Section: P, Section No. 1781, Vol. 18, No. 417, Pg. 78, August 04, 1994 (19940804)

ABSTRACT

PURPOSE: To distribute the load of a data management, and to improve the safety of data.

CONSTITUTION: Plural computers 110, 111, 112,... are logically connected in a tree structure, the computer 112,... in the lowest layer are used as working computers, and the computers 110,... in the other layers are used as management computers which manage the data of the computers in the lower layer connected with their own computers. The computers which can perform an access to the data of the management computers are limited to the computers in the lower layer and the computers in the upper layer connected with the management computers. Therefore, not only the working of a program but also the management of data can be distributed, so that the load of the computers can be reduced. Moreover, the data are multiply managed by the plural management computers, so that the loss of the data due to an accident or a willful action can be prevented.

4/5/16 (Item 16 from file: 347)
DIALOG(R)File 347:JAPIO

03893942 **Image available**
TRAIN OPERATION CONTROL SYSTEM

PUB. NO.: 04-259042 [JP 4259042 A]
PUBLISHED: September 14, 1992 (19920914)
INVENTOR(s): **TATE SEISAKU**
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-040696 [JP 9140696]
FILED: February 14, 1991 (19910214)
INTL CLASS: [5] **G06F-011/20** ; B61L-027/00; G05B-009/03
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 22.3 (MACHINERY -- Control & Regulation); 44.9 (COMMUNICATION -- Other)
JOURNAL: Section: P, Section No. 1476, Vol. 17, No. 45, Pg. 164, January 28, 1993 (19930128)

ABSTRACT

PURPOSE: To decrease the number of computers and to improve the investing efficiency by providing a common back-up device to plural routes management companies.

CONSTITUTION: A trouble monitoring device 13A monitoring totally the operation control units 11a, 11b and 11c for each of plural routes and produces the interruption signals 32a-32c at occurrence of troubles of the units 11a-11c, a back-up device 16 switching the operating programs in response to those interruption signals and backs up the operation control unit having a trouble, an information means to give the real-time operating state information to the units 11a-11c and the device 16 are provided. Thus the device 16 takes over the operating state information in place of the faulty operation control unit in order to automatically and instantaneously carry on the operation.

4/5/17 (Item 17 from file: 347)
DIALOG(R)File 347:JAPIO

03340178 **Image available**
IMAGE INPUT SYSTEM

PUB. NO.: 03-003078 [JP 3003078 A]
PUBLISHED: January 09, 1991 (19910109)
INVENTOR(s): **TATE SHIGEKI**
TAKEDA HARUO
ISE HIROTOSHI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
HITACHI MICRO COMPUT ENG LTD [470864] (A Japanese Company or

Corporatio[redacted] JP (Japan)
APPL. NO.: 01-136038 [JP 89136038]
FILED: May 31, 1989 (19890531)
INTL CLASS: [5] **G06F-015/62**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications)
JOURNAL: Section: P, Section No. 1180, Vol. 15, No. 111, Pg. 148, March 18, 1991 (19910318)

ABSTRACT

PURPOSE: To dividedly input a document whose size is larger than that of a scanner in a direction capable of easily inputting it by dividedly inputting a document, recognizing the position and direction of the inputted divided image to the whole document, and if necessary rotating the divided image in accordance with the direction.

CONSTITUTION: The image input system is provided with the scanner 1 for inputting image data, a file 3 for storing registered image data, a keyboard 7, a mouse 8, a processor (CPU) 9, image memory memos 10-1 to 10-4, 11, and so on. A document is dividedly inputted, the position and direction of the inputted divided image to the whole document are recognized, and if necessary the divided image is rotated in accordance with the direction, and the divided image is coupled with an already inputted divided image. Consequently, a document whose size is larger than that of the scanner can be dividedly inputted in the direction capable of easily inputting it.

4/5/18 (Item 18 from file: 347)
DIALOG(R)File 347:JAPIO

02981760 **Image available**
CONVERSION SYSTEM FOR DOCUMENT FORMAT

PUB. NO.: 01-279360 [JP 1279360 A]
PUBLISHED: November 09, 1989 (19891109)
INVENTOR(s): NOMURA KUNIHIRO
YAMADA NAOKI
TATE SHIGEKI
TAKEDA HARUO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
HITACHI MICRO COMPUT ENG LTD [470864] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-108999 [JP 88108999]
FILED: May 06, 1988 (19880506)
INTL CLASS: [4] **G06F-015/20**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications)
JAPIO KEYWORD:R139 (INFORMATION PROCESSING -- Word Processors)
JOURNAL: Section: P, Section No. 998, Vol. 14, No. 50, Pg. 106, January 30, 1990 (19900130)

ABSTRACT

PURPOSE: To process the document data produced by a low-function device incapable of the table processing with use of a high-function device capable of the table processing by extracting the ruled line information and defining this as a table area.

CONSTITUTION: A high-function device capable of the table processing has a data structure where the in-table data are discriminated from the out-table data and therefore reads physically the volume label of a supplied floppy disk to discriminate a specific device type that produced the document data. Then a table area is extracted out of the ruled line information in case it is known that the document is produced by such a device that controls the ruled line information and the character information independently of each other and does not define these information as a table. The character information also includes the characters contained in the table and therefore each character is checked for its specific display position in the document. Thus the characters contained in the table area

are defined as the t[redacted]e data having the coincide[redacted] with the data structure of the high-function device.

4/5/19 (Item 19 from file: 347)
DIALOG(R)File 347:JAPIO
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02161791
CONFIRMATION SELLING SYSTEM FOR RESERVED SEAT IN TRAIN

PUB. NO.: 62-078691 [JP 62078691 A]
PUBLISHED: April 10, 1987 (19870410)
INVENTOR(s): **TATE SEISAKU**
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-220593 [JP 85220593]
FILED: October 01, 1985 (19851001)
INTL CLASS: [4] G07B-001/00; **G06F-015/26**
JAPIO CLASS: 29.4 (PRECISION INSTRUMENTS -- Business Machines); 45.4 (INFORMATION PROCESSING -- Computer Applications)

4/5/20 (Item 20 from file: 347)
DIALOG(R)File 347:JAPIO
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02095555
TRAIN SERVICE CONTROL SYSTEM

PUB. NO.: 62-012455 [JP 62012455 A]
PUBLISHED: January 21, 1987 (19870121)
INVENTOR(s): **TATE SEISAKU**
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-151378 [JP 85151378]
FILED: July 11, 1985 (19850711)
INTL CLASS: [4] B61L-025/00; B61L-027/00; **G06F-015/48**
JAPIO CLASS: 44.9 (COMMUNICATION -- Other); 45.4 (INFORMATION PROCESSING -- Computer Applications)
JAPIO KEYWORD:R012 (OPTICAL FIBERS)

4/5/21 (Item 21 from file: 347)
DIALOG(R)File 347:JAPIO
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01409916 **Image available**
FUNCTION PATTERN GENERATOR

PUB. NO.: 59-121516 [JP 59121516 A]
PUBLISHED: July 13, 1984 (19840713)
INVENTOR(s): **TATE SEISAKU**
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-229753 [JP 82229753]
FILED: December 28, 1982 (19821228)
INTL CLASS: [3] **G06F-001/02**
JAPIO CLASS: 45.9 (INFORMATION PROCESSING -- Other); 26.1 (TRANSPORTATION -- Railways)
JOURNAL: Section: P, Section No. 313, Vol. 08, No. 248, Pg. 157, November 14, 1984 (19841114)

ABSTRACT
PURPOSE: To make fail-safe circuit constitution possible, by making a read-only memory parallel and dual and passing function weight data of this memory with a chip-enable signal formed with a specific weight pulse train.
CONSTITUTION: ROMs 11 and 12 where prescribed function data Q(sub 1)-Q(sub

n) are entered are arranged in parallel as a dual system and data Q(sub 1)-Q(sub n) corresponding to address inputs A(sub 1)-A(sub n) are outputed by AND between chip-enable inputs CE(sub 1) and CE(sub 2) to attain a function pattern pulse train S. A fundamental clock pulse has the frequency divided, and two synchronizing weight pulse trains P(sub 1)- P(sub n) and P(sub 1)'-P(sub n)' having a phase shift are operated in ANDs 41-44 and are inputted to respective inputs CE(sub 2) of ROMs 11 and 13 as chip-enable signals to output data Q(sub 1)-Q(sub n) whose readout is shifted from one another, and they pass SRFFs 21-2n and DTFFs 31-3n generating a phase conversion pulse and are operated in an AND 45, thus attaining the fail-safe output S.

4/5/22 (Item 22 from file: 347)

01268830 **Image available**

RESET PULSE GENERATING CIRCUIT DURING APPLICATION OF POWER SUPPLY

PUB. NO.: 58-206230 [JP 58206230 A]
PUBLISHED: December 01, 1983 (19831201)
INVENTOR(s): **TATE SEISAKU**
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-091643 [JP 8291643]
FILED: May 27, 1982 (19820527)
INTL CLASS: [3] H03K-017/22; **G06F-001/00** ; H03K-003/02
JAPIO CLASS: 42.4 (ELECTRONICS -- Basic Circuits); 45.9 (INFORMATION PROCESSING -- Other)
JOURNAL: Section: E, Section No. 231, Vol. 08, No. 53, Pg. 109, March 09, 1984 (19840309)

ABSTRACT

PURPOSE: To generate assuredly a reset pulse although a power supply is cut off or reapplied with any timing, by utilizing a general-purpose timer IC.

CONSTITUTION: The voltage of a threshold terminal (d) rises up with a time constant decided by the products of the time constant values of a resistance 23 and a capacitor 24 after a power supply 20 is applied. If the power supply voltage is set at VCC, the reference voltage at the inside of a timer IC25 is set at (2/3XVCC). Then the 1st voltage comparator 11 is inverted when (threshold voltage)>=(2/3XVCC) is satisfied. A reset input is applied to a flip-flop 13, and the output Q of the flip-flop 13 is set at 1. Then the output of a terminal (g) is also set at 1. Furthermore, the output Q is set at 1 to make a transistor TR16 conduct since terminals (d) and (h) are connected in common. At the same time, the electric charge stored in a capacitor 24 is discharged instantaneously through the TR16. Thus the voltage between both ends of the capacitor 24 is kept approximately at 0V.

4/5/23 (Item 23 from file: 347)

01115700 **Image available**

FAILURE DETECTOR FOR FUNCTION PATTERN GENERATOR

PUB. NO.: 58-053100 [JP 58053100 A]
PUBLISHED: March 29, 1983 (19830329)
INVENTOR(s): **TATE SEISAKU**
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-151825 [JP 81151825]
FILED: September 24, 1981 (19810924)
INTL CLASS: [3] G11C-029/00; **G06F-011/22** ; G11C-017/00
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.1

(INFORMATI[redacted]PROCESSING -- Arithmetic Seque[redacted]Units)
JOURNAL: Section: P, Section No. 204, Vol. 07, No. 138, Pg. 111, June 16, 1983 (19830616)

ABSTRACT

PURPOSE: To easily detect failures of a function pattern generator, by constituting a circuit so that a data used actually and a data in which each bit of one address is all 0 can alternately be stored at each one address.

CONSTITUTION: An output of an ROM 7 is provided with a logical inverting gate 8 for all 0 detection and an AND gate 9. An AND between a coincidence output A of an AND gate 10 and a failure timing signal (b) is taken at an F/F control gate F(sub 1)10 and directly coupled to a reset terminal of a flip-flop 11. An inverting output of the output A is taken as A', the A' and the (b) are ANDed at an F/F control gate F(sub 2)12 and directly connected to set terminal of the flip-flop 11. Thus, in driving the circuit, the output of the flip-flop 11 changes as 1->0-> 1->0- and an AC exciting output B is obtained, If a failure takes place, the state of AC oscillation is stopped at the output of the flip-flop 11.

4/5/24 (Item 24 from file: 347)
DIALOG(R)File 347:JAPIO

00636119 **Image available**
DATA INPUT CIRCUIT

PUB. NO.: 55-123719 [JP 55123719 A]
PUBLISHED: September 24, 1980 (19800924)
INVENTOR(s): **TATE SEISAKU**
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 54-030892 [JP 7930892]
FILED: March 15, 1979 (19790315)
INTL CLASS: [3] **G06F-003/00** ; B61L-027/00
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 26.1 (TRANSPORTATION -- Railways)
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ABSTRACT

PURPOSE: To input multi-input signals effectively by holding input signals until the completion of processing operations and by resetting preceding data when a prescribed-width notification is received.
CONSTITUTION: This circuit is constituted by adding an automatic reset circuit and a data coming signal gate C to data holding circuits 2(sub 1)-2(sub n). The reset circuit is equipped with FF,D and drives the T terminal of FF,D when coming signal P(sub 1) is outputted to a processing unit. At this time, data obtained by OR between the signal output of circuit 2(sub 1)-2(sub n) and gate E is written to the terminal of FF,D and is connected to the reset terminal of FF,D. When data comes, a pules is outputted from the preceding-stage FF of circuits 2(sub 1)-2(sub n) is outputted and becomes a notification signal and becomes a timing pulse simultaneously to operate OR among the OR output of the succeeding-stage FF, read processing completion signal P(sub 2), and gate F and reset the succeeding-stage FF by reset signal P(sub 3). Therefore, FF,D generates a differential pulse for data coming. Though the succeeding-stage FF is set for data signal 0->1, a new signal is held because the reset signal precedes this set.

4/5/25 (Item 25 from file: 347)
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MICROCOMPUTER SYSTEM

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INVENTOR(s): **TATE SEISAKU**
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
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ABSTRACT

PURPOSE: To have a supplement to the ASR typewriter function by adding a control command using the unused signal line of the interface circuit.